

DDR5 5600 REGISTERED DUAL INLINE MEMORY MODULE RDIMM

MSR64GSD55646MB4-BLK, 64GB 2Rx8 8G x 80-Bit CL46 Registered ECC 288-Pin DIMM

General Description

PNY MSR64GSD55646MB4-BLK is a 8G x 80-bit (64GB) DDR5-5600 CL46 SDRAM (Synchronous DRAM) 2Rx8, memory module, based on twenty MICRON B-die 4G x 8-bit (32Gb) FBGA components per module. Each 288-pin DIMM uses gold contact fingers.

1. Features

- Power Supply: VDD = 1.1V Typical
- VDDQ = 1.1V Typical
- VPP = 1.8V Typical
- VDDSPD = 1.8V to 2.0V
- On-Die ECC
- x80 ECC (x40, 2 independent I/O sub channels)
- 32 internal bank
- 8 bank group
- Based on 4Gbx8 SDRAM Components (Micron B-die)
- Module Rank = 2 Rank

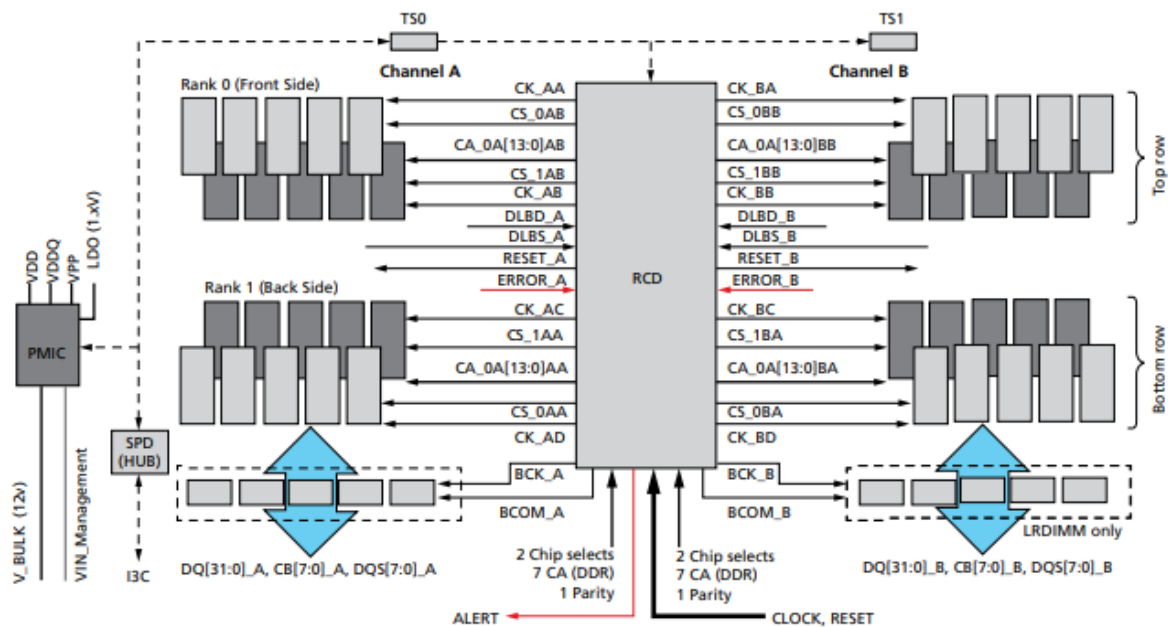
2. Specifications

- CL (IDD) 46 cycles
- Row Cycle Time (tRCmin) 48.0ns (min.)
- Row to Column Delay (tRCDmin) 16.0ns (min.)
- Row Precharge time (tRPmin) 16.0ns (min.)
- Row Active time (tRASmin) 32.00ms (min.)
- UL Rating 94 V – 0
- Operating Temperature 0°C to +85°C
- Storage Temperature -55°C to +100°C

3. Timing Parameters

Default (JEDEC) DDR5-5600 CL46-45-45@1.1V

4. Block Diagram



Note: 1. The above illustrates a dual-rank x80 LRDIMM/RDIMM with DRAM, PMIC, RCD, SPD, temp sensors and data buffers.

5. Pin Assignment

Pin#	Front Side	Pin#	Front Side	Pin#	Front Side	Pin#	Front Side	Pin#	Back Side	Pin#	Back Side	Pin#	Back Side	Pin#	Back Side
1	VIN_BULK	37	VSS	73	VSS	109	DQ5_B	145	VIN_BULK	181	DQ22_A	217	CK_t	253	VSS
2	RFU	38	DQ21_A	74	PAR_A	110	VSS	146	VIN_BULK	182	VSS	218	CK_C	254	DQ7_B
3	VIN_MGMT	39	VSS	75	VSS	111	DQ8_B	147	PCAMP	183	DQ23_A	219	VSS	255	VSS
4	HSCL	40	DQ24_A	76	CA0_B	112	VSS	148	HAS	184	VSS	220	RFU	256	DQ10_B
5	HSDA	41	VSS	77	VSS	113	DQ9_B	149	RFU	185	DQ26_A	221	CA1_B	257	VSS
6	VSS	42	DQ25_A	78	CA2_B	114	VSS	150	RFU	186	VSS	222	VSS	258	DQ11_B
7	DQ0_A	43	VSS	79	VSS	115	DQS1_B_t	151	VSS	187	DQ27_A	223	CA3_B	259	VSS
8	VSS	44	DQS3_A_t	80	CA4_B	116	DQS1_B_c	152	DQ2_A	188	VSS	224	VSS	260	DQS6_A_c, TDQS6_A_c
9	DQ1_A	45	DQS3_A_c	81	VSS	117	VSS	153	VSS	189	DQS8_A_c, TDQS8_A_c	225	CA5_B	261	DQS6_A_t, TDQS6_A_t
10	VSS	46	VSS	82	CA6_B	118	DQ12_B	154	DQ3_A	190	DQS8_A_t, TDQS8_A_t	226	VSS	262	VSS
11	DQS0_A_t	47	DQ28_A	83	VSS	119	VSS	155	VSS	191	VSS	227	PAR_B	263	DQ14_B
12	DQS0_A_c	48	VSS	84	CS0_B_n	120	DQ13_B	156	DQS5_A_c, TDQS5_A_c	192	DQ30_A	228	VSS	264	VSS
13	VSS	49	DQ29_A	85	VSS	121	VSS	157	DQS5_A_t, TDQS5_A_t	193	VSS	229	CS1_B_n	265	DQ15_B
14	DQ4_A	50	VSS	86	DLBDQ	122	DQ16_B	158	VSS	194	DQ31_A	230	VSS	266	VSS
15	VSS	51	CB0_A	87	DLBDQS	123	VSS	159	DQ6_A	195	VSS	231	RFU	267	DQ18_B
16	DQ5_A	52	VSS	88	VSS	124	DQ17_B	160	VS	196	CB2_A	232	RFU	268	VSS
17	VSS	53	CB1_A	89	CB4_B	125	VSS	161	DQ7_A	197	VSS	233	VSS	269	DQ19_B
18	DQ8_A	54	VSS	90	VSS	126	DQS2_B_t	162	VSS	198	CB3_A	234	CB6_B	270	VSS
19	VSS	55	DQS4_A_t	91	CB5_B	127	DQS2_B_c	163	DQ10_A	199	VSS	235	VSS	271	DQS7_A_c, TDQS7_A_c
20	DQ9_A	56	DQS4_A_c	92	VSS	128	VSS	164	VSS	200	DQS9_A_c, TDQS9_A_c	236	CB7_B	272	DQS7_A_t, TDQS7_A_t
21	VSS	57	VSS	93	DQS9_B_t, TDQS9_B_t	129	DQ20_B	165	DQ11_A	201	DQS9_A_t, TDQS9_A_t	237	VSS	273	VSS
22	DQS1_A_t	58	CB4_A	94	DQS9_B_c, TDQS9_B_c	130	VSS	166	VSS	202	VSS	238	DQS4_B_c	274	DQ22_B
23	DQS1_A_c	59	VSS	95	VSS	131	DQ21_B	167	DQS6_A_c, TDQS6_A_c	203	CB6_A	239	DQS4_B_t	275	VSS
24	VSS	60	CB5_A	96	CB0_B	132	VSS	168	DQS6_A_t, TDQS6_A_t	204	VSS	240	VSS	276	DQ23_B
25	DQ12_A	61	VSS	97	VSS	133	DQ24_B	169	VSS	205	CB7_A	241	CB2_B	277	VSS
26	VSS	62	ALERT_n	98	CB1_B	134	VSS	170	DQ14_A	206	VSS	242	VSS	278	DQ26_B
27	DQ13_A	63	VSS	99	VSS	135	DQ25_B	171	VSS	207	RESET_n	243	CB3_B	279	VSS
28	VSS	64	CS0_A_n	100	DQ0_B	136	VSS	172	DQ15_A	208	VSS	244	VSS	280	DQ27_B
29	DQ16_A	65	VSS	101	VSS	137	DQS3_B_t	173	VSS	209	CS1_A_n	245	DQ2_B	281	VSS
30	VSS	66	CA0_A	102	DQ1_B	138	DQS3_B_c	174	DQ18_A	210	VSS	246	VSS	282	DQS8_A_c, TDQS8_A_c
31	DQ17_A	67	VSS	103	VSS	139	VSS	175	VSS	211	CA1_A	247	DQ3_B	283	DQS8_A_t, TDQS8_A_t
32	VSS	68	CA2_A	104	DQS0_B_t	140	DQ28_B	176	DQ19_A	212	VSS	248	VSS	284	VSS
33	DQS2_A_t	69	VSS	105	DQS0_B_c	141	VSS	177	VSS	213	CA3_A	249	DQS5_A_c, TDQS5_A_c	285	DQ30_B
34	DQS2_A_c	70	CA4_A	106	VSS	142	DQ29_B	178	DQS7_A_c, TDQS7_A_c	214	VSS	250	DQS5_A_t, TDQS5_A_t	286	VSS
35	VSS	71	VSS	107	DQ4_B	143	VSS	179	DQS7_A_t, TDQS7_A_t	215	CA5_A	251	VSS	287	DQ31_B
36	DQ20_A	72	CA6_A	108	VSS	144	RFU	180	VSS	216	VSS	252	DQ6_B	288	VSS

6. Pin Descriptions

Pin	Description	Function
CA[6:0]_A CA[6:0]_B	Address and Command Bus	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during Mode Register Set commands.
CS[1:0]_A CS[1:0]_B	Chip Select	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command codes. CS_n is also used to enter and exit the parts from power down mode and self-refresh mode. While not in self-refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self-refresh the CS_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
PAR_A PAR_B	Parity input	Each Command Address input parity is received on the DPAR pin and should maintain even parity across the channel CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
CK_t	Clocks (true/positive)	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CK_c	Clocks (complement/negative)	
ALERT_n	Alert for CRC error	Alert: If there is an error in CRC, then ALERT_n shall drive LOW for the period time interval and return HIGH. During Connectivity Test mode, this pin functions as an input. Usage of this signal or not is system dependent. In case this pin is not connected, ALERT_n pin must be bonded to VDDQ on the system board.
RESET_n	Set DRAM to known state	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
PCAMP	Control and Monitor Port	Control and Monitor Port. Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).
HSCL	I2C/I3C-Basic Host Sideband Bus Clock	Bus clock used to strobe data into HUB device. When open drain, a pullup resistor is required on the system motherboard.
HSDA	I2C/I3C-Basic Host Sideband Bus Data	I2C/I3C-Basic data. When Open drain, a pullup resistor is required on the system motherboard.
HSA	I2C/I3C-Basic Host Sideband Bus Address	Device address for the HUB. Tied to GND through resistor for HID in normal operation and directly to GND in tester operation
DLBDQ	Loopback Data output:	Loopback Data output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled the pin is either terminated or Hi-Z based on MR36: OP[2:0].
DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A & B	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A & B	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used - for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating
DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended.
DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)	
TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Not used on LRDIMMs.
TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.	
VIN_BULK	DIMM Power Supply from system to PMIC	External power supply: 12 V, 4.25 V (min), 15 V (max).
VIN_MGMT	DIMM Power Supply from system to PMIC	External power supply: 3.3 V, 3.0 V (min), 3.6 V (max).
VSS	Power supply return (ground)	Ground
RFU	Reserved for future use	Reserved for Future Use: No on DIMM electrical connection is present.
DLBDQS	Loopback Data strobe output	Loopback Data Strobe output: This is a single ended strobe with the rising edged aligned with Loopback Data edge, falling edge aligned with Data center. When Loopback is enabled it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or Hi-Z based on MR36: OP[2:0].

Note 1 TDQSx and DQSx_t share a pin.

7. Absolute Maximum Ratings

Registering Clock Driver

Symbol	Parameter	Min	Max	Units
V _{DD}	Supply voltage	-0.3	1.4	V
V _{IN}	Receiver input voltage	-0.3	V _{DD} + 0.5	V
V _{OUT}	Driver output voltage	-0.3	V _{DD} + 0.5	V
I _{IK}	Input clamp current	-	-50	mA
I _{OK}	Output clamp current	-	±50	mA
I _{OUT}	Continuous output current	-	±50	mA
I _{CCC}	Continuous current through each V _{DD} or V _{SS} pin	-	±100	mA
T _{stg}	Storage temperature	-55	100	°C

PMIC Input Supply Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bulk input supply voltage – DC voltage	VIN_Bulk	4.25	12	15	V	1, 2
Bulk input supply maximum – AC voltage	VIN_Bulk_AC	-	-	18	V	
Bulk input supply maximum voltage – start up overshoot	VIN_Bulk_OS_Startup	-	-	33	V*μs	3
Bulk input supply voltage – ramp up rate	VIN_Bulk_Ramp_Up	0.1	-	3	V/ms	4
Bulk input supply voltage – ramp down rate	VIN_Bulk_Ramp_Down	-	-	1	V/ms	5
Management input supply voltage	VIN_Mgmt	3	3.3	3.6	V	6
Management input supply – ramp up and ramp down rate	VIN_Mgmt_Ramp	0.15	-	3	V/ms	
Minimum management input supply current	IVIN_Mgmt	110	-	-	mA	7
Bulk input supply current	IVIN_Bulk	-	-	2.5	A	8

- Notes:
1. During first power on, the input voltage supply must reach minimum value based on default from register 0x1A [7:5] + 1.0V for PMIC to detect valid input supply. Refer to the JEDEC PMIC50x0 specification for register implementation detail.
 2. The PMIC efficiency is optimized for nominal input supply of 12V or lower. The PMIC efficiency above 13.8V is degraded and thermal impact must be considered. The PMIC operation above 14.2V should not be greater than 20% duty cycle at any time and should be limited to a maximum contiguous period of 10 minutes.
 3. The area under the curve above VIN_Bulk = 15V. VIN_Bulk_AC spec must also be satisfied.
 4. The ramp up rate between 300mV and 8.0V.
 5. The ramp down rate between 8.0V and 300mV.
 6. During first power-on, the input voltage supply must reach minimum value of 2.8V for PMIC to detect valid input supply.
 7. This is a platform specification. It is the minimum input current delivered by the platform through the DIMM gold finger to deliver the maximum load on LDO outputs (1.8V LDO output + 1.0V LDO output = 25mA + 20mA) plus the current required by the PMIC for its own usage.
 8. This is a platform specification. It is the maximum input current delivered by the platform through the DIMM gold fingers.

Operation Temperature Condition

Symbol	Parameter/Condition	Value	Units	Notes
T _C	DRAM Commercial operating case temperature	0 to 85	°C	1, 2, 3
T _C		>85 to 95	°C	1, 2, 3, 4
T _{OPER}	DRAM operating temperature range	0 to 95	°C	5, 7, 8
T _{STG}	DRAM Non-operating storage temperature	-55 to 100	°C	6

- Notes:
1. Maximum operating case temperature; TC is measured in the center of the package.
 2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum TC during operation.
 3. Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.
 4. If TC exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95μs interval refresh rate.

5. The refresh rate must double when $85^{\circ}\text{C} < \text{TC} \leq 95^{\circ}\text{C}$.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.
7. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C and 85°C under all operating conditions for the commercial offering.

8. DC Operating Condition

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz		Notes
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit	
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	10	mOhm	20	mOhm	3

Note 1: VDD must be written 66mv of VDDQ.

Note 2: AC parameters are measured with VDD and VDDQ tied together.

Note 3: This includes all voltage noise from DC to 2Mhz at the DRAM package ball.

9. IDD Specification

Parameter	Symbol	5600	6400	7200	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}^1	205	216	TBD	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}^1	246	250	TBD	mA
Precharge standby current	I_{DD2N}^2	203	218	TBD	mA
Precharge standby non-target command	I_{DD2NT}^1	243	258	TBD	mA
Precharge power-down current	I_{DD2P}^2	179	192	TBD	mA
Active standby current	I_{DD3N}^2	232	242	TBD	mA
Active power-down current	I_{DD3P}^2	207	214	TBD	mA
Operating burst read current	I_{DD4R}^1	484	526	TBD	mA
Operating burst write current	I_{DD4W}^1	615	671	TBD	mA
Operating burst write with write CRC current	I_{DD4WC}^1	570	613	TBD	mA
Burst refresh (normal refresh mode) current	I_{DD5B}^1	486	486	TBD	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}^1	464	464	TBD	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}^1	272	278	TBD	mA
Self refresh current	I_{DD6N}^2	101	101	TBD	mA
Operating bank interleave read current	I_{DD7}^1	647	723	TBD	mA
Maximum power saving deep power down mode current	I_{DD8}^2	172	172	TBD	mA

Note 1: One module rank in this $I_{DD}/I_{DDQ}/I_{PP}$ condition, the other rank in I_{DD2N}/I_{PP2N} .

Note 2: Both ranks in this $I_{DD}/I_{DDQ}/I_{PP}$ condition.

10. Timing Measurement

Speed Bin CL-nRCD-nRP					DDR5-5600 46-45-45		Unit
Parameter				Symbol	min		
Read command to first data				tAA	16.000	ns	
Activate to Read or Write command delay time				tRCD	16.000	ns	
Row Precharge time				tRP	16.000	ns	
Activate to Precharge command period				tRAS	32.000	ns	
Activate to Activate or Refresh command period				tRC (tRAS+tRP)	48.000	ns	
CAS Write Latency				CWL	CL-2	nCK	
Speed Bins	tAAmin (ns)	tRCDmin / tRP min (ns)	Read CL	Supported Frequency Down Bins			
5600	16.000	16.000	46	tCK(AVG)	0.357	ns	
Supported CL					22,28,32,36,40,42	nCK	

11. Outline Drawing

