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Less Heat, Less Power Consumption

STABLE
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Stable and
Reliable Solution

Server/Workstation
Motherboard

TURIN2D24G-2L+
GENOA2D24G-2L+

User Manual

English

Version 2.00
Published Nov. 2024

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"Perchlorate Material-special handling may apply, see www.dtsc.ca.gov/hazardouswaste/perchlorate"

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This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

ASRock Rack INC. hereby declares that this device is in compliance with the essential requirements and other relevant provisions of related UKCA Directives. Full text of UKCA declaration of conformity is available at: http://www.asrockrack.com

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ASRock Rack follows the green design concept to design and manufacture our products, and makes sure that each stage of the product life cycle of ASRock Rack product is in line with global environmental regulations. In addition, ASRock Rack disclose the relevant information based on regulation requirements.

Please refer to https://www.asrockrack.com/general/about.asp?cat=Responsibility for information disclosure based on regulation requirements ASRock Rack is complied with:

DO NOT throw the motherboard in municipal waste. This product has been designed to enable proper reuse of parts and recycling. This symbol of the crossed out wheeled bin indicates that the product (electrical and electronic equipment) should not be placed in municipal waste. Check local regulations for disposal of electronic products.

Contents

Chapter 1 Introduction

Thank you for purchasing ASRock Rack ***TURIN2D24G-2L+ / GENOA2D24G-2L+*** motherboard, a reliable motherboard produced under ASRock Rack's consistently stringent quality control. It delivers excellent performance with robust design conforming to ASRock Rack's commitment to quality and endurance.

In this manual, chapter 1 and 2 contains introduction of the motherboard and step-by-step guide to the hardware installation. Chapter 3 and 4 contains the configuration guide to BIOS setup and information of the Sofware Support.

Because the motherboard specifications and the BIOS software might be updated, the content of this manual will be subject to change without notice. In case any modifications of this manual occur, the updated version will be available on ASRock Rack website without further notice. Find the latest memory and CPU support lists on ASRock Rack website as well. ASRock Rack's Website: www.ASRockRack.com

For any technical supports, please visit the website for specific information about the using model. http://www.asrockrack.com/support/

1.1 Package Contents

- ASRock Rack TURIN2D24G-2L+ / GENOA2D24G-2L+ motherboard (Proprietary form factor: 16.9" x 13.8", 42.9cm x 35.1cm)
- Quick installation guide
- 1 x ATX 4P to 24P power cable (8cm)
- 2 x screws for M.2 sockets

If any items are missing or appear damaged, contact the authorized dealer.

English

1.2 Specifications

TURIN2D24G-2L+ / GENOA2D24G-2L+	
Physical Status	
Form Factor	Proprietary
Dimension	16.9" x13.8"
Processor System	
CPU	Supports AMD EPYC™ 9005*/9004 (with AMD 3D V-Cache™ Technology) and 97x4 series processors
**For GENOA2D24G-2L+, a BIOS update is required to support AMD EPYC™ 9005 series processors*	
Socket	Dual Socket SP5 (LGA6096)
Thermal Design Power (TDP)	**GENOA2D24G-2L+:** Up to 400W **TURIN2D24G-2L+:** Up to 500W
Chipset	System on Chip
System Memory	
Supported DIMM Quantity	12+12 DIMM slots (1DPC)
Supported Type	Supports DDR5 288-pin RDIMM, RDIMM-3DS
Max. Capacity per DIMM	RDIMM: up to 96GB (2R) 3DS RDIMM: up to 512GB (2S8RX4)
Max. Frequency	**GENOA2D24G-2L+:** 4800MHz **TURIN2D24G-2L+:** 6000MHz (For EPYC 9005 series processors) 4800MHz (For EPYC 9004 series processors)
Voltage	1.1V
Note	*Memory capacity, frequency, or voltage support is to be validated*
SATA/SAS Storage	
CPU Built-in Storage	AMD EPYC™ 9005/9004 (Up to 32 SATA 6Gb/s): 4 MCIO
Additional SATA Controller	ASM1061 (2 SATA 6Gb/s): 2 M.2
Ethernet	
Additional GbE Controller	Intel® i350: 2 RJ45 (1GbE)
Other PCIe Expansion Connectors	
M.2 Slot	M2_1 (PCIe3.0 x4 or SATA 6Gb/s), supports 2280/22110 form factor [CPU0] M2_2 (PCIe3.0 x4 or SATA 6Gb/s), supports 2280/22110 form factor [CPU1]

MCIO	**GENOA2D24G-2L+:** 6 MCIO (PCIe5.0 / CXL1.1 x8) [CPU0] 2 MCIO (PCIe5.0 / CXL1.1 x8 or 8 SATA 6Gb/s) [CPU0] 2 MCIO (PCIe5.0 x8 or 8 SATA 6Gb/s) [CPU0]* 6 MCIO (PCIe5.0 / CXL1.1 x8) [CPU1] 2 MCIO (PCIe5.0 / CXL1.1 x8 or 8 SATA 6Gb/s) [CPU1] 2 MCIO (PCIe5.0 x8) [CPU1] **TURIN2D24G-2L+:** 6 MCIO (PCIe5.0 / CXL2.0 x8) [CPU0] 2 MCIO (PCIe5.0 / CXL2.0 x8 or 8 SATA 6Gb/s) [CPU0] 2 MCIO (PCIe5.0 x8 or 8 SATA 6Gb/s) [CPU0]* 6 MCIO (PCIe5.0 / CXL2.0 x8) [CPU1] 2 MCIO (PCIe5.0 / CXL2.0 x8 or 8 SATA 6Gb/s) [CPU1] 2 MCIO (PCIe5.0 x8) [CPU1]
**MCIO9, 10 support PCIe only while installing 2 processors*	
Server Management	
BMC Controller	ASPEED AST2600
IPMI Dedicated GLAN	1 Realtek RTL8211F for dedicated management GLAN
Graphics	
Controller	ASPEED AST2600
VRAM	DDR4 512MB
Security	
TPM	1 (13-pin, SPI)
Rear I/O	
UID Button/LED	1 UID button w/ LED
Other Button/LED	1 PWR button, 1 RST button, 1 NMI button, 1 HDD LED, 1 SYS LED
VGA Port	1 DB15 (VGA)
USB	4 Type-A (USB3.2 Gen1)
RJ45	2 RJ45 (1GbE), 1 dedicated IPMI
Hardware Monitor	
Temperature	CPU, MB, Card side Temperature Sensing
Fan	Fan Tachometer CPU Quiet Fan (Allow Chassis Fan Speed Auto-Adjust by CPU Temperature) Fan Multi-Speed Control
Voltage	P0_VDDCR_CPU0, P0_VDDCR_CPU1, P0_VDDCR_SOC, P0_VDD_18_DUAL, P0_VDD_11_S3, P0_VDDIO, P1_VDDCR_CPU0, P1_VDDCR_CPU1, P1_VDDCR_SOC, P1_VDD_18_DUAL, P1_VDD_11_S3, P1_VDDIO, +BAT, +12V, +3VSB, +5VSB

System BIOS	
Type	AMI UEFI BIOS; 256 Mb (32MB) SPI Flash ROM
Features	ASRock Rack Instant Flash, ACPI 6.4 and about compliance wake up events, SMBIOS 3.5.0 and above, Plug and Play(PnP)
Internal Connectors/Headers	
PSU Connector	6 Micro-Hi (8-pin, ATX 12V), 1 Micro-Fit (4-pin, ATX PSU signal) w/ ATX 24-pin adapter cable, 1 (2-pin, +5V)
Auxiliary Panel Header	1 (18-pin): chassis intrusion, system fault LED, LAN1/LAN2 activity LED, locate, SMBus
System Panel Header	1 (9-pin): power switch, reset switch, system power LED, HDD activity LED
NMI Button	1
COM Header	1
VGA Header	1
Fan Header	6 (6-pin)
TPM Header	1 (13-pin,SPI)
SGPIO Header	6
HSBP	1
SMbus Header	4
PMbus Header	1
IPMB Header	1
Clear CMOS	1 (contact pads)
USB 3.2 (Gen1) Header	2 (19-pin, 2 USB3.2 Gen1)
LED Indicators	
Standby Power LED	1 (5VSB)
80 Debug Port LED	1
Fan Fail LED	6
BMC Heartbeat LED	1
Support OS	
OS	Microsoft® Windows®: - Server 2019 (64bit) - Server 2022 (64bit) - Server 2025 (64bit) Linux®: - RedHat Enterprise Linux Server 8.10 (64bit) / Server 9.5 (64bit) - SUSE SLES 15.5(64bit) / 15.6(64bit) - UBuntu 22.04.5 (64bit) / 24.04 (64bit) Hypervisor: - VMWare ESXi / 8.0 U3 / 9.0 **Please refer to the website for the latest OS support list.*

Enviroment	
Operating temperature	10 - 35°C (50 - 95degF)
Non-operating temperature	-40 - 70°C (-40 - 158degF)

NOTE: Please refer to the website for the latest specifications.

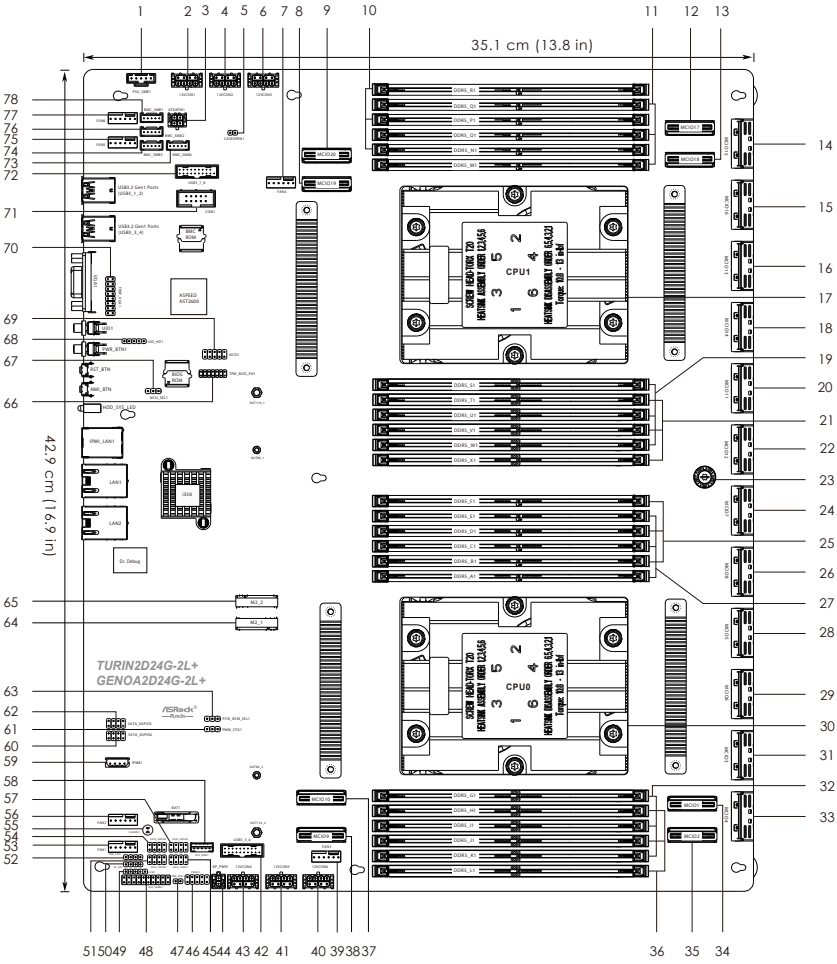
This motherboard supports Wake from on Board LAN. To use this function, please make sure that the "Wake on Magic Packet from power off state" is enabled in Device Manager > Intel® Ethernet Connection > Power Management. And the "PCI Devices Power On" is enabled in UEFI SETUP UTILITY > Advanced > ACPI Configuration. After that, onboard LAN1&2 can wake up S5 under OS.

If installing Intel® LAN utility or Marvell SATA utility, this motherboard may fail Windows® Hardware Quality Lab (WHQL) certification tests. If installing the drivers only, it will pass the WHQL tests.

1.3 Unique Features

ASRock Rack Instant Flash is a BIOS flash utility embedded in Flash ROM. This convenient BIOS update tool allows user to update system BIOS without entering operating systems first like MS-DOS or Windows®. With this utility, press the <F6> key during the POST or the <F2> key to enter into the BIOS setup menu to access ASRock Rack Instant Flash. Just launch this tool and save the new BIOS file to the USB flash drive, floppy disk or hard drive, then updating the BIOS only in a few clicks without preparing an additional floppy diskette or other complicated flash utility. Please be noted that the USB flash drive or hard drive must use FAT32/16/12 file system.

1.4 Motherboard Layout



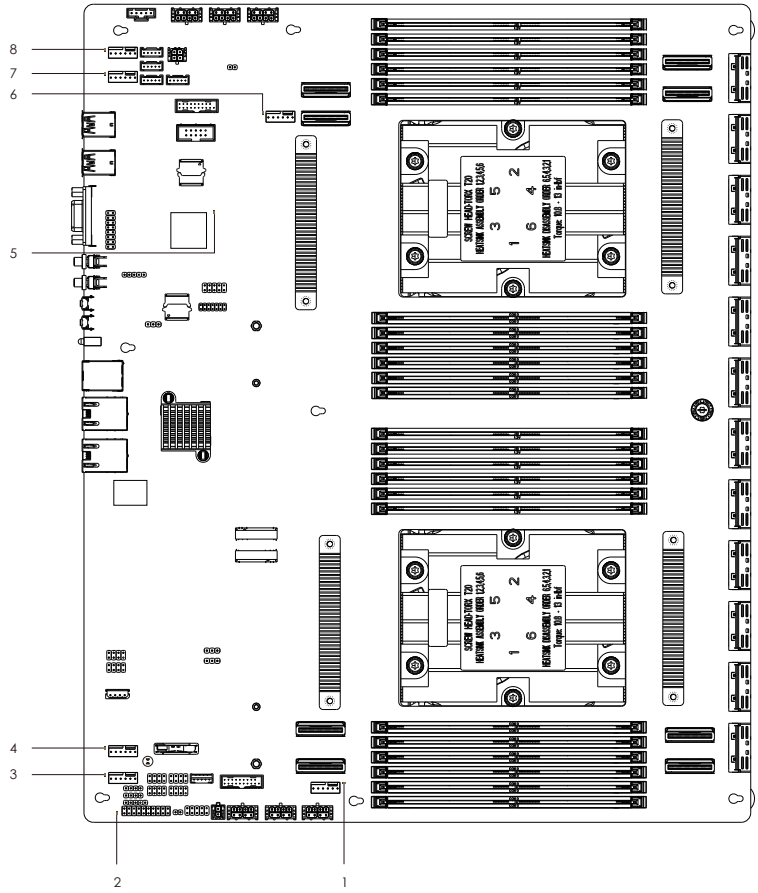
No.	Description
1	PSU SMBus Header (PSU_SMB1)
2	ATX 12V Power Connector (12VCON1)
3	Micro-Fit Power Connector (ATX4PIN1)
4	ATX 12V Power Connector (12VCON2)
5	Chassis Intrusion Header (CASEOPEN1)
6	ATX 12V Power Connector (12VCON3)
7	System Fan Connector (FAN4)
8	Mini Cool Edge IO Connector (MCIO19)
9	Mini Cool Edge IO Connector (MCIO20)
10	3 x 288-pin DDR5 DIMM Slots (DDR5_N1, DDR5_P1, DDR5_R1)*
11	3 x 288-pin DDR5 DIMM Slots (DDR5_M1, DDR5_O1, DDR5_Q1)*
12	Mini Cool Edge IO Connector (MCIO17)
13	Mini Cool Edge IO Connector (MCIO18)
14	Mini Cool Edge IO Connector (MCIO15)
15	Mini Cool Edge IO Connector (MCIO16)
16	Mini Cool Edge IO Connector (MCIO13)
17	AMD Socket SP5 (SM-LGA-6096) (CPU1)
18	Mini Cool Edge IO Connector (MCIO14)
19	3 x 288-pin DDR5 DIMM Slots (DDR5_S1, DDR5_U1, DDR5_W1)*
20	Mini Cool Edge IO Connector (MCIO11)
21	3 x 288-pin DDR5 DIMM Slots (DDR5_T1, DDR5_V1, DDR5_X1)*
22	Mini Cool Edge IO Connector (MCIO12)
23	Thumbscrew
24	Mini Cool Edge IO Connector (MCIO7)
25	3 x 288-pin DDR5 DIMM Slots (DDR5_B1, DDR5_D1, DDR5_F1)*
26	Mini Cool Edge IO Connector (MCIO8)
27	3 x 288-pin DDR5 DIMM Slots (DDR5_A1, DDR5_C1, DDR5_E1)*
28	Mini Cool Edge IO Connector (MCIO5)
29	Mini Cool Edge IO Connector (MCIO6)
30	AMD Socket SP5 (SM-LGA-6096) (CPU0)
31	Mini Cool Edge IO Connector (MCIO3)
32	3 x 288-pin DDR5 DIMM Slots (DDR5_G1, DDR5_I1, DDR5_K1)*
33	Mini Cool Edge IO Connector (MCIO4)
34	Mini Cool Edge IO Connector (MCIO1)

No.	Description
35	Mini Cool Edge IO Connector (MCIO2)
36	3 x 288-pin DDR5 DIMM Slots (DDR5_H1, DDR5_J1, DDR5_L1)*
37	Mini Cool Edge IO Connector (MCIO10)
38	Mini Cool Edge IO Connector (MCIO9)
39	System Fan Connector (FAN3)
40	ATX 12V Power Connector (12VCON6)
41	ATX 12V Power Connector (12VCON5)
42	USB 3.2 Gen1 Header (USB3_5_6)
43	ATX 12V Power Connector (12VCON4)
44	System Power Connector (BP_PWR1)
45	SATA SGPIO Connector (SATA_SGPIO1)
46	System Panel Header (PANEL1)
47	Non Maskable Interrupt Button (NMI_BTN1)
48	Auxiliary Panel Header (AUX_PANEL1)
49	Liquid Crystal Module Header (LCM1)
50	Rear Panel LAN LED (RL_LED)
51	SATA SGPIO Connector (SATA_SGPIO3)
52	IPMI LAN LED Header (IPMI_LED1)
53	System Fan Connector (FAN1)
54	SATA SGPIO Connector (SATA_SGPIO4)
55	Clear CMOS Pad (CLRMOS1)
56	System Fan Connector (FAN2)
57	SATA SGPIO Connector (SATA_SGPIO2)
58	Backplane PCI Express Hot-Plug Connector (CPU_HSBP1)
59	Intelligent Platform Management Bus Header (IPMB1)
60	SATA SGPIO Connector (SATA_SGPIO6)
61	PWM Configuration Header (PWM_CFG1)
62	SATA SGPIO Connector (SATA_SGPIO5)
63	PCIE Signal Source Selection Jumper (PCIE_BCM_SEL1)
64	M.2 Socket (M2_1) (Type 2280/22110)
65	M.2 Socket (M2_2) (Type 2280/22110)
66	SPI TPM Header (TPM_BIOS_PH1)
67	NCSI Mode Jumper (NCSI_SEL1)
68	UID Button Header (UID_HD1)

No.	Description
69	NCSI Header (NCSI1)
70	Front VGA Header (FRNT_VGA1)
71	COM Port Header (COM1)
72	USB 3.2 Gen1 Header (USB3_7_8)
73	BMC SMBus Header (BMC_SMB4)
74	BMC SMBus Header (BMC_SMB3)
75	System Fan Connector (FAN5)
76	BMC SMBus Header (BMC_SMB2)
77	System Fan Connector (FAN6)
78	BMC SMBus Header (BMC_SMB1)

* *For DIMM installation and configuration instructions, please see p.20 (Installation of Memory Modules (DIMM)) for more details.*

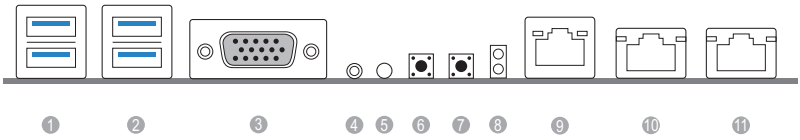
1.5 Onboard LED Indicators



No.	Item	Status	Description
1	LED_FAN3	Red	FAN3 failed
2	SB_PWR1	Green	STB PWR ready
3	LED_FAN1	Red	FAN1 failed
4	LED_FAN2	Red	FAN2 failed
5	BMC_LED1	Green	BMC heartbeat LED
6	LED_FAN4	Red	FAN4 failed
7	LED_FAN5	Red	FAN5 failed
8	LED_FAN6	Red	FAN6 failed

English

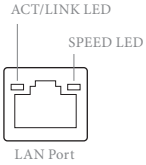
1.6 I/O Panel



No.	Description	No.	Description
1	USB 3.2 Gen1 Ports (USB3_1_2)	7	NMI Button (NMI_BTN)
2	USB 3.2 Gen1 Ports (USB3_3_4)	8	HDD/System Fault LED (HDD_SYS_LED)
3	VGA Header (VGA1)	9	IPMI LAN Header (IPMI_LAN1)*
4	UID Switch (UID1)	10	1G LAN RJ-45 Port (LAN1, shared NIC)**
5	Power Switch/LED (PWR_BTN1)	11	1G LAN RJ-45 Port (LAN2)**
6	Reset Button (RST_BTN)		

LAN Port LED Indications

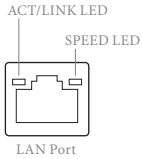
*There is an LED on each side of IPMI LAN port. Please refer to the table below for the LAN port LED indications.



IPMI LAN Port LED Indications

Activity / Link LED		Speed LED	
Status	Description	Status	Description
Off	No Link	Off	10Mbps connection or no link
Blinking Yellow	Data Activity	Orange	100Mbps connection
On	Link	Green	1Gbps connection

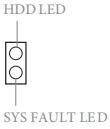
**There is an LED on each side of 1G LAN port. Please refer to the table below for the LAN port LED indications.



1G LAN Port (LAN1, LAN2) LED Indications

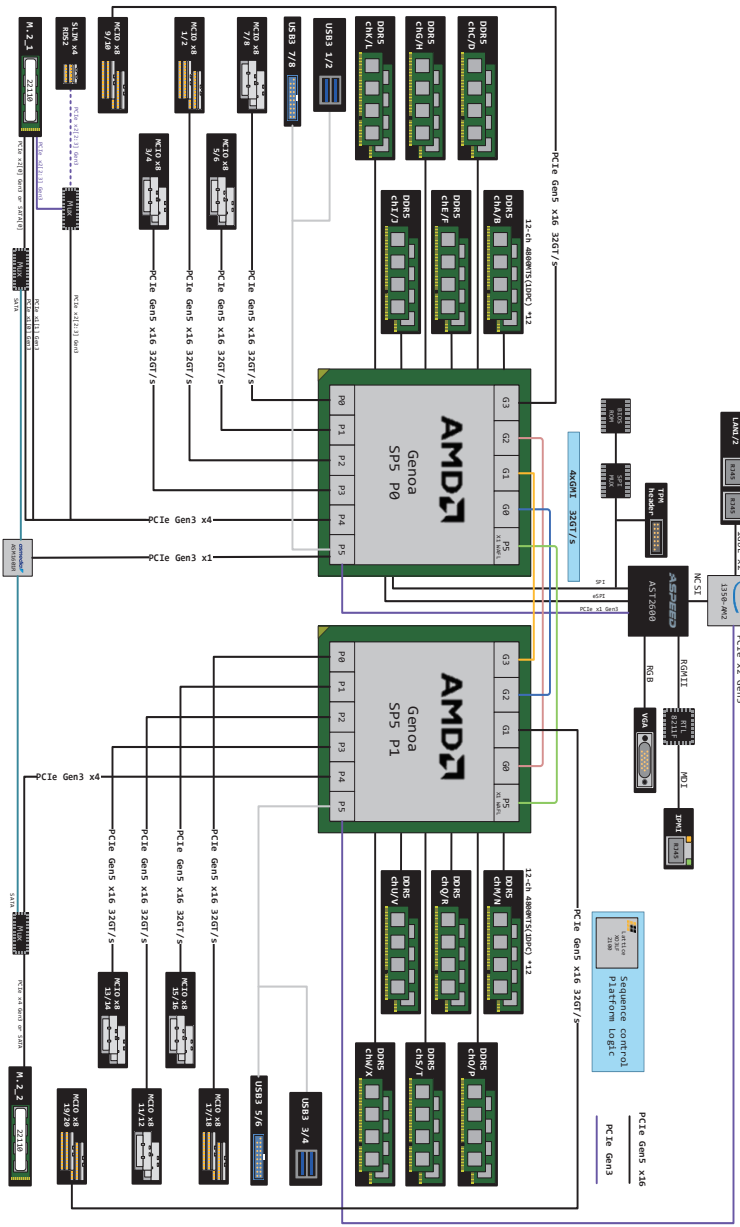
Activity / Link LED		Speed LED	
Status	**Description**	**Status**	**Description**
Off	No Link	Off	10Mbps connection or no link
Blinking Yellow	Data Activity	Orange	100Mbps connection
On	Link	Green	1Gbps connection

HDD/System Fault LED Indications



HDD LED		SYS FAULT LED	
Status	**Description**	**Status**	**Description**
Off	HDD inactive	Off	Normal
Green	HDD active	RED	System Fault

1.7 Block Diagram



English

Chapter 2 Installation

This is a Proprietary form factor (18.93" x13.78") motherboard. Before installing the motherboard, study the configuration of the chassis to ensure that the motherboard fits into it.

Make sure to unplug the power cord before installing or removing the motherboard. Failure to do so may cause physical injuries and motherboard damages.

2.1 Screw Holes

Place screws into the holes indicated by circles to secure the motherboard to the chassis.

Do not over-tighten the screws! Doing so may damage the motherboard.

2.2 Pre-installation Precautions

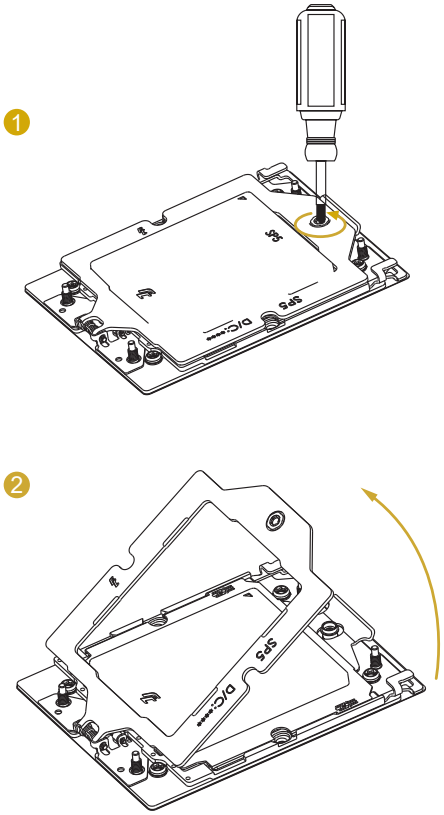
Take note of the following precautions before installing motherboard components or change any motherboard settings.

1. Unplug the power cord from the wall socket before touching any components.
2. To avoid damaging the motherboard's components due to static electricity, NEVER place the motherboard directly on the carpet or the like. Also remember to use a grounded wrist strap or touch a safety grounded object before handling the components.
3. Hold components by the edges and do not touch the ICs.
4. Whenever uninstall any component, place it on a grounded anti-static pad or in the bag that comes with the component.
5. When placing screws into the screw holes to secure the motherboard to the chassis, please do not over-tighten the screws! Doing so may damage the motherboard.

Before installing or removing any component, ensure that the power is switched off or the power cord is detached from the power supply. Failure to do so may cause severe damage to the motherboard, peripherals, and/or components.

2.3 Installing the CPU

1. *Before inserting the CPU into the socket, please check if the PnP cap is on the socket, if the CPU surface is unclean, or if there are any bent pins in the socket. Do not force to insert the CPU into the socket if above situation is found. Otherwise, the CPU will be seriously damaged.*
2. *Unplug all power cables before installing the CPU.*



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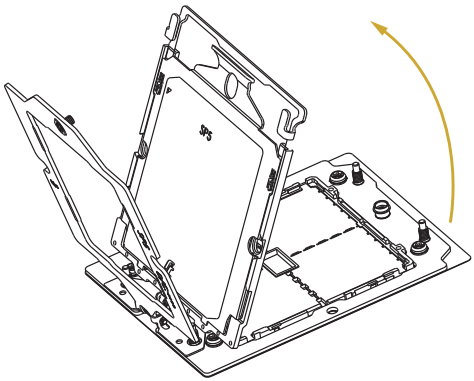

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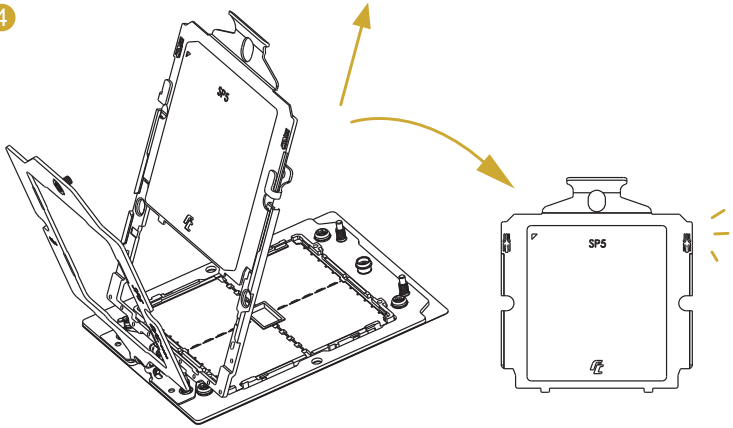

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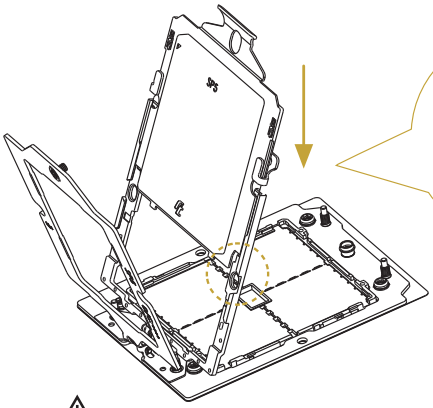
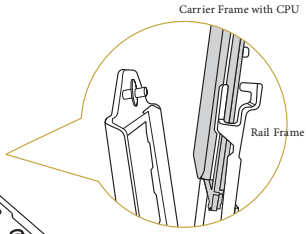
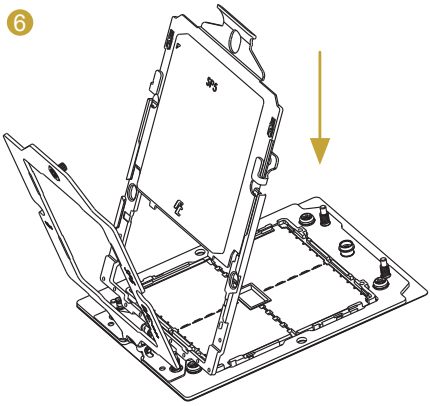




Please make sure that the carrier frame with CPU is closely attached to the rail frame while inserting it.

⚠ Install the carrier frame with CPU. Don't separate them.

6



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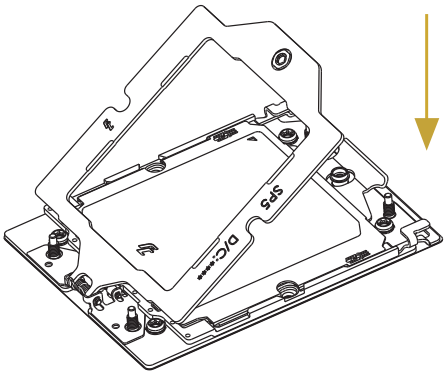

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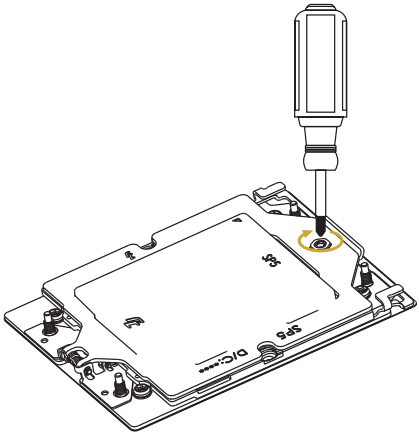
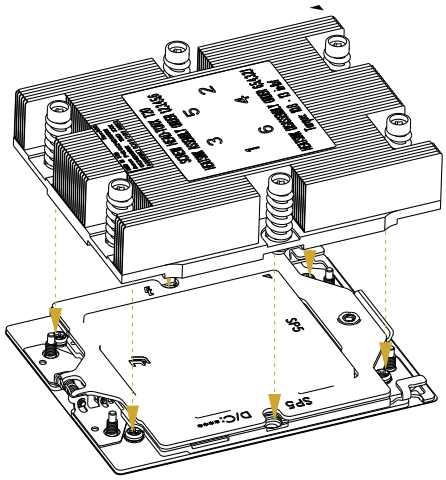
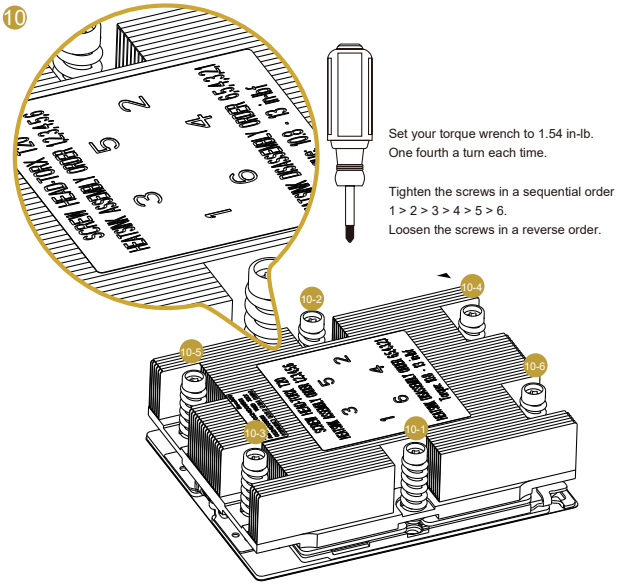


9



10



Set your torque wrench to 1.54 in-lb.
One fourth a turn each time.

Tighten the screws in a sequential order
1 > 2 > 3 > 4 > 5 > 6.
Loosen the screws in a reverse order.

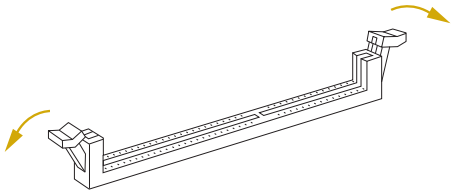
2.4 Installation of Memory Modules (DIMM)

This motherboard provides twenty-four 288-pin DDR5 (Double Data Rate 5) DIMM slots in two groups, and supports Single Channel Memory Technology.

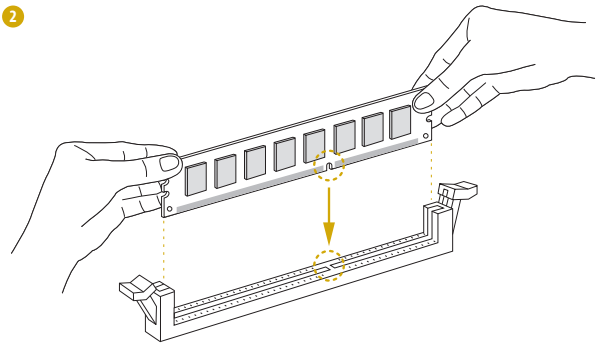
CPU1	CPU0
DDR5_M1, N1, O1, P1, Q1, R1	DDR5_A1, B1, C1, D1, E1, F1
DDR5_S1, T1, U1, V1, W1, X1	DDR5_G1, H1, I1, J1, K1, L1

1. *It is not allowed to install a DDR, DDR2, DDR3 or DDR4 memory module into a DDR5 slot; otherwise, this motherboard and DIMM may be damaged.*
2. *For Single channel configuration, it always needs to install identical (the same brand, speed, size and chip-type) DDR5 DIMMs.*

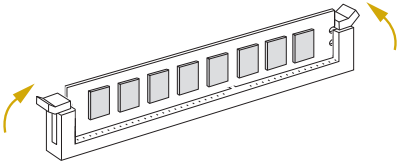
1



2



3

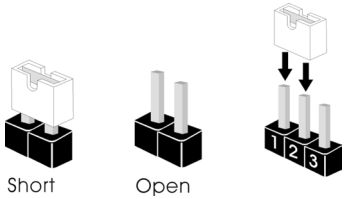


Recommended Memory Configurations

Number of Memory Channels Populated	Number of CPU Installed	AMD Recommended Memory Channels																							
		CPU0												CPU1											
		A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	K1	L1	M1	N1	O1	P1	Q1	R1	S1	T1	U1	V1	W1	X1
24	2P	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	1P																								
20	2P	V	V	V	V	V		V	V	V	V	V		V	V	V	V	V		V	V	V	V	V	
	1P																								
16	2P	V	V	V		V		V	V	V		V		V	V	V		V		V	V	V		V	
	1P																								
12	2P	V	V	V				V	V	V				V	V	V				V	V	V			
	1P	V	V	V	V	V	V	V	V	V	V	V	V												
10	2P																								
	1P	V	V	V	V	V		V	V	V	V	V													
8	2P	V		V				V		V				V		V				V		V			
	1P	V	V	V		V		V	V	V		V													
6	2P																								
	1P	V	V	V				V	V	V															
4	2P	V						V						V						V					
	1P	V		V				V		V															
2	2P	V												V											
	1P	V						V																	
1	2P																								
	1P	V																							

2.5 Jumper Setup

The illustration shows how jumpers are setup. When the jumper cap is placed on the pins, the jumper is "Short". If no jumper cap is placed on the pins, the jumper is "Open". The illustration shows a 3-pin jumper whose pin1 and pin2 are "Short" when a jumper cap is placed on these 2 pins.



NCSI Mode Jumper (3-pin NCSI_SEL1) (see p.6, No. 67)	1_2 NCSI to I350 (Default)	2_3 NCSI to NCSI Header (NCSI1)
PCIE Signal Source Selection Jumper (3-pin PCIE_BCM_SEL1) (see p.6, No. 63)	1_2 RDS2 + M.2_1 (x2)	2_3 M.2_1 (x4) (Default)

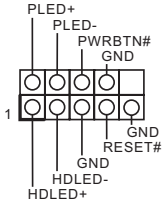
RDS2 shares singal source with M.2_1:
1. RDS2 is PCIe3.0 x2 when M2_1 supports only PCIe3.0 x2 or SATA 6Gb/s
2. RDS2 is no function when M2_1 supports PCIe3.0 x4 or SATA 6Gb/s

English

2.6 Onboard Headers and Connectors

Onboard headers and connectors are NOT jumpers. Do NOT place jumper caps over these headers and connectors. Placing jumper caps over the headers and connectors will cause permanent damage to the motherboard.

System Panel Header
(9-pin PANEL1)
(see p.6, No.46)



Connect the power switch, reset switch and system status indicator on the chassis to this header according to the pin assignments. Particularly note the positive and negative pins before connecting the cables.

PWRBTN (Power Switch):
Connect to the power switch on the chassis front panel. It may configure the way to turn off the system using the power switch.

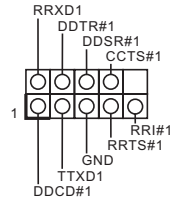
RESET (Reset Switch):
Connect to the reset switch on the chassis front panel. Press the reset switch to restart the computer if the computer freezes and fails to perform a normal restart.

PLED (System Power LED):
Connect to the power status indicator on the chassis front panel. The LED is on when the system is operating. The LED is off when the system is in S4 sleep state or powered off (S5).

HDLED (Hard Drive Activity LED):
Connect to the hard drive activity LED on the chassis front panel. The LED is on when the hard drive is reading or writing data.

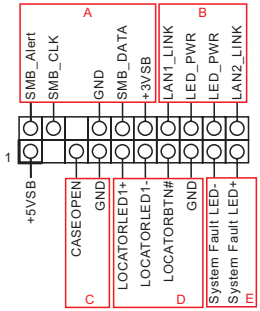
The front panel design may differ by chassis. A front panel module mainly consists of power switch, reset switch, power LED, hard drive activity LED, speaker and etc. When connecting the chassis front panel module to this header, make sure the wire assignments and the pin assignments are matched correctly.

Serial Port Header
(9-pin COM1)
(see p.6, No. 71)



This COM header supports a serial port module.

Auxiliary Panel Connector
(18-pin AUX_PANEL1)
(see p.6, No. 48)



This header supports multiple functions on the front panel, including front panel SMB, internet status indicator.

A. Front panel SMBus connecting pin (6-1 pin FPSMB)
This header allows user to connect SMBus (System Management Bus) equipment. It can be used for communication between peripheral equipment in the system, which has slower transmission rates, and power management equipment.

B. Internet status indicator (2-pin LAN1_LED, LAN2_LED)
These two 2-pin headers allow user to use the Gigabit internet indicator cable to connect to the LAN status indicator. When this indicator flickers, it means that the internet is properly connected.

C. Chassis intrusion pin (2-pin CHASSIS)
This header is provided for host computer chassis with chassis intrusion detection designs. In addition, it must also work with external detection equipment, such as a chassis intrusion detection sensor or a microswitch. When this function is activated, if any chassis component movement occurs, the sensor will immediately detect it and send a signal to this header, and the system will then record this chassis intrusion event. The default setting is set to the CASEOPEN and GND pin; this function is off.

D. Locator LED (4-pin LOCATOR)
This header is for the locator switch and LED on the front panel.

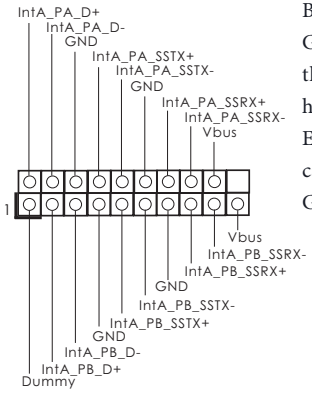
E. System Fault LED (2-pin LOCATOR)
This header is for the Fault LED on the system.

Non Maskable Interrupt
Button Header
(2-pin NMI_BTN1)
(see p.6, No. 47)

Please connect a NMI device to this header.

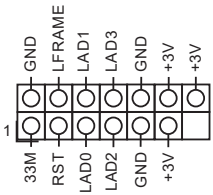
English

USB 3.2 Gen1 Headers
(19-pin USB3_5_6)
(see p.6, No. 42)
(19-pin USB3_7_8)
(see p.6, No. 72)



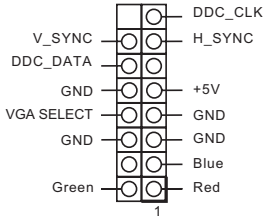
Besides four default USB 3.2 Gen1 ports on the I/O panel, there are two USB 3.2 Gen1 headers on this motherboard. Each USB 3.2 Gen1 header can support two USB 3.2 Gen1 ports.

SPI TPM Header
(13-pin TPM_BIOS_PH1)
(see p.6, No. 66)



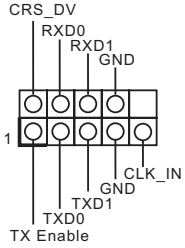
This connector supports SPI Trusted Platform Module (TPM) system, which can securely store keys, digital certificates, passwords, and data. A TPM system also helps enhance network security, protects digital identities, and ensures platform integrity.

Front VGA Header
(15-pin FRNT_VGA1)
(see p.6, No. 70)



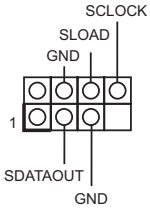
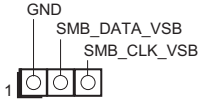
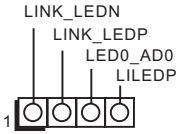
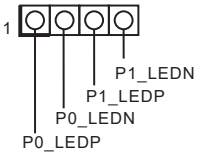
Please connect either end of the VGA cable to this VGA header.

NCSI Header
(9-pin NCSI1)
(see p.6, No. 69)

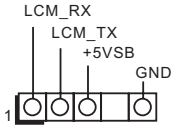


The onboard NCSI header is used for external connections.

English

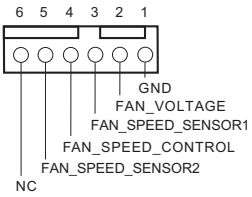
Serial General Purpose Input/Output Headers (7-pin SATA_SGPIO1) (see p.6, No. 45) (7-pin SATA_SGPIO2) (see p.6, No. 57) (7-pin SATA_SGPIO3) (see p.6, No. 51) (7-pin SATA_SGPIO4) (see p.6, No. 54) (7-pin SATA_SGPIO5) (see p.6, No. 62) (7-pin SATA_SGPIO6) (see p.6, No. 60)		These headers support Serial Link interface for onboard SATA connections.
PWM Configuration Header (3-pin PWM_CFG1) (see p.6, No. 61)		This header is used for PWM configurations.
IPMI LAN LED Header (4-pin IPMI_LED1) (see p.6, No. 52)		This header is used to connect to the LED indicators on the chassis.
Rear Panel LAN LED (4-pin RL_LED) (see p.6, No. 50)		This header is used for extended LAN LED on the rear panel of a server system.
Chassis Intrusion Header (2-pin CASEOPEN1) (see p.6, No. 5)		This motherboard supports CASE OPEN detection feature that detects if the chassis cover has been removed. This feature requires a chassis with chassis intrusion detection design.

Liquid Crystal Module Header
(4-pin LCM1)
(see p.6, No. 49)



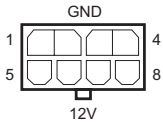
This header is used for extended Liquid Crystal Module(LCM) on the front panel of a server system.

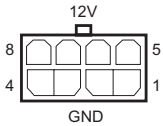
System Fan Connectors
(6-pin FAN1)
(see p.6, No. 53)
(6-pin FAN2)
(see p.6, No. 56)
(6-pin FAN3)
(see p.6, No. 39)
(6-pin FAN4)
(see p.6, No. 7)
(6-pin FAN5)
(see p.6, No. 75)
(6-pin FAN6)
(see p.6, No. 77)



Please connect fan cables to the fan connectors and match the black wire to the ground pin. All fans support Fan Control.

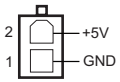
ATX 12V Power Connectors
(8-pin 12VCON1)
(see p.6, No. 2)
(8-pin 12VCON2)
(see p.6, No. 4)
(8-pin 12VCON3)
(see p.6, No. 6)
(8-pin 12VCON4)
(see p.6, No. 43)
(8-pin 12VCON5)
(see p.6, No. 41)
(8-pin 12VCON6)
(see p.6, No. 40)





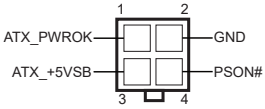
This motherboard provides six ATX power connectors.

System Power Connector
(2-pin BP_PWR1)
(see p.6, No. 44)



This motherboard provides one +5V power connector for system configuration.

Micro-Fit ATX 4Pin Power Connector (4-pin ATX4PIN1 (ATX 24pin-to-4pin)) (see p.6, No. 3)



The motherboard provides one 4-pin power/signal connector which is a required input for ATX power source. When using ATX power, it is necessary to use a 24pin-to-4pin power cable to connect between the 24pin power connector of PSU and the 12VCON1~6 connectors on the motherboard for power supply and signal communication

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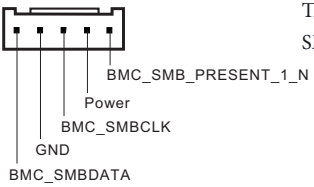
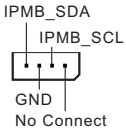
BMC SMB Headers
(5-pin BMC_SMB1) (see p.6, No. 78)
(5-pin BMC_SMB2) (see p.6, No. 76)
(5-pin BMC_SMB3) (see p.6, No. 74)
(5-pin BMC_SMB4) (see p.6, No. 73)

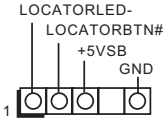
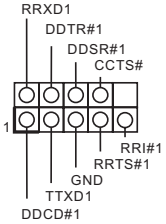
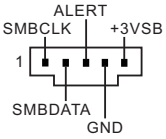
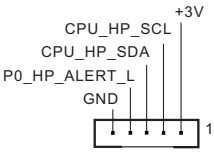


These headers are used for the SMBUS devices.

Intelligent Platform Management Bus header (4-pin IPMB1) (see p.6, No. 59)



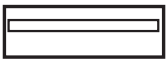
This 4-pin connector is used to provide a cabled baseboard or front panel connection for value added features and 3rd-party add-in cards, such as Emergency Management cards, that provide management features using the IPMB.

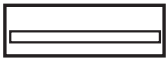
UID Header (4-pin UID_HD) (see p.6, No. 68)		This 4-pin header is used for the Unit Identification LED and switch functions.
COM Port Header (9-pin COM1) (see p.6, No. 71)		This COM header supports a serial port module.
PSU SMBus (PSU_SMB1) (see p.6, No. 1)		PSU SMBus monitors the status of the power supply, fan and system temperature.
Backplane PCI Express Hot-Plug Connector (5-pin CPU_ HSBP1) (see p.6, No. 58)		This header is used for the hot plug feature of HDDs on the backplane.
Clear CMOS Pad (CLRMOS1) (see p.6, No. 55)		This allows user to clear the data in CMOS. To clear CMOS, take out the CMOS battery and short the Clear CMOS Pad.

MCIO Connectors
(MCIO1)
(see p.6, No. 34)
(MCIO2)
(see p.6, No. 35)
(MCIO9)
(see p.6, No. 38)
(MCIO10)
(see p.6, No. 37)
(MCIO17)
(see p.6, No. 12)
(MCIO18)
(see p.6, No. 13)
(MCIO19)
(see p.6, No. 8)
(MCIO20)
(see p.6, No. 9)

Right Angle

(MCIO3)
(see p.6, No. 31)
(MCIO4)
(see p.6, No. 33)
(MCIO5)
(see p.6, No. 28)
(MCIO6)
(see p.6, No. 29)
(MCIO7)
(see p.6, No. 24)
(MCIO8)
(see p.6, No. 26)
(MCIO11)
(see p.6, No. 20)
(MCIO12)
(see p.6, No. 22)
(MCIO13)
(see p.6, No. 16)
(MCIO14)
(see p.6, No. 18)
(MCIO15)
(see p.6, No. 14)
(MCIO16)
(see p.6, No. 15)





These connectors are used for the PCIE or SATA devices.

** MCIO9, 10 support PCIe only while installing 2 processors*

MCIO1 Pin Definition (CPU0 P2 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO2 Pin Definition (CPU0 P2 [15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO3 Pin Definition (CPU0 P3 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO4 Pin Definition (CPU0 P3 [15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO5 Pin Definition (CPU0 P1 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO6 Pin Definition (CPU0 P1 [15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO7 Pin Definition (CPU0 P0 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO8 Pin Definition (CPU0 P0 [15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO9 Pin Definition (CPU0 G3 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO10 Pin Definition (CPU0 G3 [15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO11 Pin Definition (CPU1 P2 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO12 Pin Definition (CPU1 P2 [15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO13 Pin Definition (CPU1 P3 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO14 Pin Definition (CPU1 P3 [15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO15 Pin Definition (CPU1 P1 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO16 Pin Definition (CPU1 P1 [15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO17 Pin Definition (CPU1 P0 [7:0])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DP7
A3	RX_DN7	B3	TX_DN7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DP6
A6	RX_DN6	B6	TX_DN6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DP5
A15	RX_DN5	B15	TX_DN5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DP4
A18	RX_DN4	B18	TX_DN4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DP3
A21	RX_DN3	B21	TX_DN3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DP2
A24	RX_DN2	B24	TX_DN2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DP1
A33	RX_DN1	B33	TX_DN1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DP0
A36	RX_DN0	B36	TX_DN0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO18 Pin Definition (CPU1 P0[15:8])

Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DP15
A3	RX_DN15	B3	TX_DN15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DP14
A6	RX_DN14	B6	TX_DN14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DP13
A15	RX_DN13	B15	TX_DN13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DP12
A18	RX_DN12	B18	TX_DN12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DP11
A21	RX_DN11	B21	TX_DN11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DP10
A24	RX_DN10	B24	TX_DN10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DP9
A33	RX_DN9	B33	TX_DN9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DP8
A36	RX_DN8	B36	TX_DN8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO19 Pin Definition (CPU1 G1 [7:0])

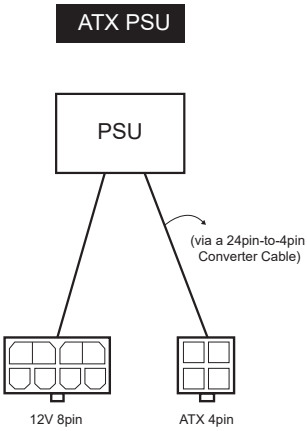
Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP7	B2	TX_DN7
A3	RX_DN7	B3	TX_DP7
A4	GND	B4	GND
A5	RX_DP6	B5	TX_DN6
A6	RX_DN6	B6	TX_DP6
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP5	B14	TX_DN5
A15	RX_DN5	B15	TX_DP5
A16	GND	B16	GND
A17	RX_DP4	B17	TX_DN4
A18	RX_DN4	B18	TX_DP4
A19	GND	B19	GND
A20	RX_DP3	B20	TX_DN3
A21	RX_DN3	B21	TX_DP3
A22	GND	B22	GND
A23	RX_DP2	B23	TX_DN2
A24	RX_DN2	B24	TX_DP2
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP1	B32	TX_DN1
A33	RX_DN1	B33	TX_DP1
A34	GND	B34	GND
A35	RX_DP0	B35	TX_DN0
A36	RX_DN0	B36	TX_DP0
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

MCIO20 Pin Definition (CPU1 G1[15:8])

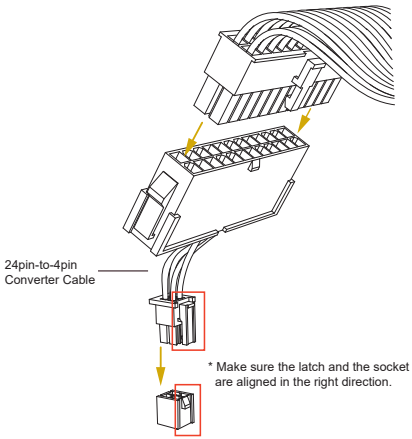
Pin	Defeinition	Pin	Defeinition
A1	GND	B1	GND
A2	RX_DP15	B2	TX_DN15
A3	RX_DN15	B3	TX_DP15
A4	GND	B4	GND
A5	RX_DP14	B5	TX_DN14
A6	RX_DN14	B6	TX_DP14
A7	GND	B7	GND
A8	BP_TYPE	B8	SCL1
A9	WAKE#	B9	SDA1
A10	GND	B10	GND
A11	DP1	B11	PERST_BUF1_N
A12	DN1	B12	PRSNT_N
A13	GND	B13	GND
A14	RX_DP13	B14	TX_DN13
A15	RX_DN13	B15	TX_DP13
A16	GND	B16	GND
A17	RX_DP12	B17	TX_DN12
A18	RX_DN12	B18	TX_DP12
A19	GND	B19	GND
A20	RX_DP11	B20	TX_DN11
A21	RX_DN11	B21	TX_DP11
A22	GND	B22	GND
A23	RX_DP10	B23	TX_DN10
A24	RX_DN10	B24	TX_DP10
A25	GND	B25	GND
A26	BP_TYPE	B26	SCL2
A27	WAKE#	B27	SDA2
A28	GND	B28	GND
A29	DP2	B29	PERST_BUF2_N
A30	DN2	B30	PRSNT_N
A31	GND	B31	GND
A32	RX_DP9	B32	TX_DN9
A33	RX_DN9	B33	TX_DP9
A34	GND	B34	GND
A35	RX_DP8	B35	TX_DN8
A36	RX_DN8	B36	TX_DP8
A37	GND	B37	GND
75	NP_NC_1	76	NP_NC_2
77	PGND_1	78	PGND_3
79	PGND_2	80	PGND_4

2.7 ATX PSU Power Connections

This motherboard support ATX power input. Please refer to the table below for the required connections between the motherboard and the power supply.



The following diagram illustrates how to connect the bundled ATX 24pin-to-4pin converter cable.



2.8 Dr. Debug

Dr. Debug is used to provide code information, which makes troubleshooting even easier. Please see the diagrams below for reading the Dr. Debug codes.

Code	Description
0x10	PEI_CORE_STARTED
0x11	PEI_CAR_CPU_INIT
0x15	PEI_CAR_NB_INIT
0x19	PEI_CAR_SB_INIT
0x31	PEI_MEMORY_INSTALLED
0x32	PEI_CPU_INIT
0x33	PEI_CPU_CACHE_INIT
0x34	PEI_CPU_AP_INIT
0x35	PEI_CPU_BSP_SELECT
0x36	PEI_CPU_SMM_INIT
0x37	PEI_MEM_NB_INIT
0x3B	PEI_MEM_SB_INIT
0x4F	PEI_DXE_IPL_STARTED
0x60	DXE_CORE_STARTED
0x61	DXE_NVRAM_INIT
0x62	DXE_SBRUN_INIT

0x63	DXE_CPU_INIT
0x68	DXE_NB_HB_INIT
0x69	DXE_NB_INIT
0x6A	DXE_NB_SMM_INIT
0x70	DXE_SB_INIT
0x71	DXE_SB_SMM_INIT
0x72	DXE_SB_DEVICES_INIT
0x78	DXE_ACPI_INIT
0x79	DXE_CSM_INIT
0x90	DXE_BDS_STARTED
0x91	DXE_BDS_CONNECT_DRIVERS
0x92	DXE_PCI_BUS_BEGIN
0x93	DXE_PCI_BUS_HPC_INIT
0x94	DXE_PCI_BUS_ENUM
0x95	DXE_PCI_BUS_REQUEST_RESOURCES
0x96	DXE_PCI_BUS_ASSIGN_RESOURCES
0x97	DXE_CON_OUT_CONNECT
0x98	DXE_CON_IN_CONNECT

0x99	DXE_SIO_INIT
0x9A	DXE_USB_BEGIN
0x9B	DXE_USB_RESET
0x9C	DXE_USB_DETECT
0x9D	DXE_USB_ENABLE
0xA0	DXE_IDE_BEGIN
0xA1	DXE_IDE_RESET
0xA2	DXE_IDE_DETECT
0xA3	DXE_IDE_ENABLE
0xA4	DXE_SCSI_BEGIN
0xA5	DXE_SCSI_RESET
0xA6	DXE_SCSI_DETECT
0xA7	DXE_SCSI_ENABLE
0xA8	DXE_SETUP_VERIFYING_PASSWORD
0xA9	DXE_SETUP_START
0xAB	DXE_SETUP_INPUT_WAIT
0xAD	DXE_READY_TO_BOOT
0xAE	DXE_LEGACY_BOOT

0xAF	DXE_EXIT_BOOT_SERVICES
0xB0	RT_SET_VIRTUAL_ADDRESS_MAP_BEGIN
0xB1	RT_SET_VIRTUAL_ADDRESS_MAP_END
0xB2	DXE_LEGACY_OPROM_INIT
0xB3	DXE_RESET_SYSTEM
0xB4	DXE_USB_HOTPLUG
0xB5	DXE_PCI_BUS_HOTPLUG
0xB6	DXE_NVRAM_CLEANUP
0xB7	DXE_CONFIGURATION_RESET
0xF0	PEI_RECOVERY_AUTO
0xF1	PEI_RECOVERY_USER
0xF2	PEI_RECOVERY_STARTED
0xF3	PEI_RECOVERY_CAPSULE_FOUND
0xF4	PEI_RECOVERY_CAPSULE_LOADED
0xE0	PEI_S3_STARTED
0xE1	PEI_S3_BOOT_SCRIPT
0xE2	PEI_S3_VIDEO_REPOST

0xE3	PEI_S3_OS_WAKE
0x50	PEI_MEMORY_INVALID_TYPE
0x53	PEI_MEMORY_NOT_DETECTED
0x55	PEI_MEMORY_NOT_INSTALLED
0x57	PEI_CPU_MISMATCH
0x58	PEI_CPU_SELF_TEST_FAILED
0x59	PEI_CPU_NO_MICROCODE
0x5A	PEI_CPU_ERROR
0x5B	PEI_RESET_NOT_AVAILABLE
0xD0	DXE_CPU_ERROR
0xD1	DXE_NB_ERROR
0xD2	DXE_SB_ERROR
0xD3	DXE_ARCH_PROTOCOL_NOT_AVAILABLE
0xD4	DXE_PCI_BUS_OUT_OF_RESOURCES
0xD5	DXE_LEGACY_OPROM_NO_SPACE
0xD6	DXE_NO_CON_OUT
0xD7	DXE_NO_CON_IN

0xD8	DXE_INVALID_PASSWORD
0xD9	DXE_BOOT_OPTION_LOAD_ERROR
0xDA	DXE_BOOT_OPTION_FAILED
0xDB	DXE_FLASH_UPDATE_FAILED
0xDC	DXE_RESET_NOT_AVAILABLE
0xE8	PEI_MEMORY_S3_RESUME_FAILED
0xE9	PEI_S3_RESUME_PPI_NOT_FOUND
0xEA	PEI_S3_BOOT_SCRIPT_ERROR
0xEB	PEI_S3_OS_WAKE_ERROR

2.9 Identification purpose LED/Switch

With the UID button, it is able to locate the server that is working on from behind a rack of servers.

Unit Identification purpose LED/Switch (UID1)		When the UID button on the front or rear panel is pressed, the front/rear UID blue LED indicator will be truned on. Press the UID button again to turn off the indicator.
Power Switch (PWR_BTN1)		Power Switch allows users to quickly turn on/off the system.

1. Press and hold the UID button for 4 seconds, the BMC will trigger an external reset.
2. Press and hold the UID button for 10 seconds, the BMC will reset and load default values.

2.10 Dual LAN and Teaming Operation Guide

Dual LAN with Teaming enabled on this motherboard allows two single connections to act as one single connection(s) for twice the transmission bandwidth, making data transmission more effective and improving the quality of transmission of distant images. Fault tolerance on the dual LAN network prevents network downtime by transferring the workload from a failed port to a working port.

The speed of transmission is subject to the actual network environment or status even with Teaming enabled.

Before setting up Teaming, please make sure whether the Switch (or Router) supports Teaming (IEEE 802.3ad Link Aggregation). Specify a preferred adapter in Intel PROSet. Under normal conditions, the Primary adapter handles all non-TCP/IP traffic. The Secondary adapter will receive fallback traffic if the primary fails. If the Preferred Primary adapter fails, but is later restored to an active status, control is automatically switched back to the Preferred Primary adapter.

Step 1

From **Device Manager**, open the properties of a team.

Step 2

Click the **Settings** tab.

Step 3

Click the **Modify Team** button.

Step 4

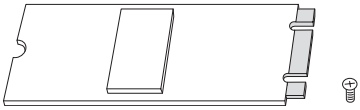
Select the adapter that want to be the primary adapter and click the **Set Primary** button.

If not specify a preferred primary adapter, the software will choose an adapter of the highest capability (model and speed) to act as the default primary. If a failover occurs, another adapter becomes the primary. The adapter will, however, rejoin the team as a non-primary.

2.11 M.2 SSD Module Installation Guide

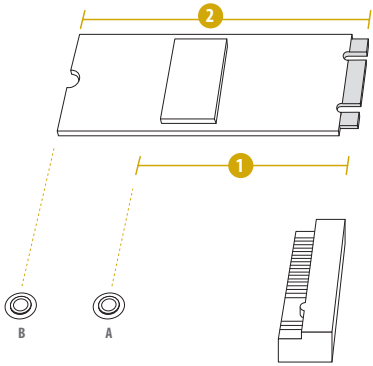
The M.2 Socket (M2_1/M2_2, Key M) supports either a M.2 SATA3.6.0 Gb/s module or a M.2 PCI Express moduel up to Gen3x4 (8Gb/s x4).

Installing the M.2 SSD Module



Step 1

Prepare a M.2 SSD module and the screw.



Step 2

Depending on the PCB type and length of the M.2 SSD module, find the corresponding nut location to be used.

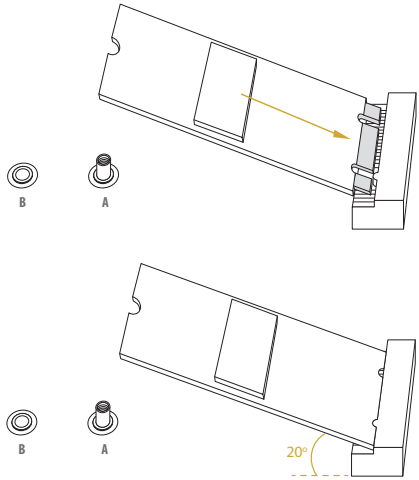
No.	2	3
Nut Location	A (NUT80_1/2)	B (NUT110_1/2)
PCB Length	8cm	11cm
Module Type	Type2280	Type22110

Step 3

Move the standoff based on the module type and length.
Skip Step 3 and 4 and go straight to Step 5 if using the default nut. Otherwise, release the standoff by hand.

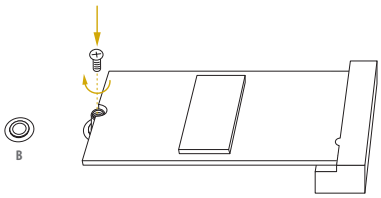
Step 4

Peel off the yellow protective film on the nut to be used. Hand tighten the standoff into the desired nut location on the motherboard.



Step 5

Align and gently insert the M.2 SSD module into the M.2 slot. Please be aware that the M.2 SSD module only fits in one orientation.



Step 6

Tighten the screw with a screwdriver to secure the module into place. Please do not overtighten the screw as this might damage the module.

Chapter 3 UEFI Setup Utility

3.1 Introduction

This section explains how to use the UEFI SETUP UTILITY to configure the system. The UEFI chip on the motherboard stores the UEFI SETUP UTILITY. Run the UEFI SETUP UTILITY when starting up the computer. Please press <F2> or <Del> during the Power-On-Self-Test (POST) to enter the UEFI SETUP UTILITY; otherwise, POST will continue with its test routines.

Restart the system by pressing <Ctrl> + <Alt> + <Delete> to enter the UEFI SETUP UTILITY after POST, or by pressing the reset button on the system chassis. This allows user to restart by turning the system off and then back on.

Because the UEFI software is constantly being updated, the following UEFI setup screens and descriptions are for reference purpose only, and they may not exactly match what seeing on the screen.

3.1.1 UEFI Menu Bar

The top of the screen has a menu bar with the following selections:

Item	Description
Main	To set up the system time/date information
Advanced	To set up the advanced UEFI features
Security	To set up the security features
Server Mgmt	To manage the server
Event Logs	For event log configuration
Boot	To set up the default system device to locate and load the Operating System
Exit	To exit the current screen or the UEFI SETUP UTILITY

Use < ← > key or < → > key to choose among the selections on the menu bar, and then press <Enter> to get into the sub screen.

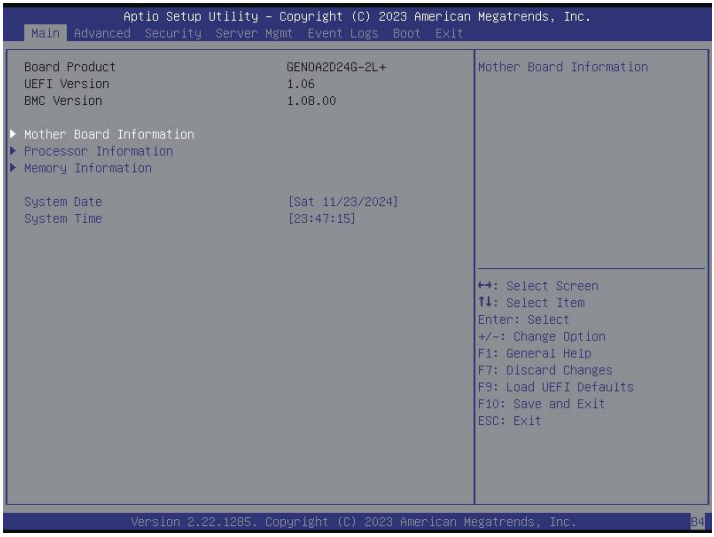
3.1.2 Navigation Keys

Please check the following table for the function description of each navigation key.

Navigation Key(s)	Function Description
← / →	Moves cursor left or right to select Screens
↑ / ↓	Moves cursor up or down to select items
+ / -	To change option for the selected items
<Tab>	Switch to next function
<Enter>	To bring up the selected screen
<PGUP>	Go to the previous page
<PGDN>	Go to the next page
<HOME>	Go to the top of the screen
<END>	Go to the bottom of the screen
<F1>	To display the General Help Screen
<F7>	Discard changes and exit the UEFI SETUP UTILITY
<F9>	Load optimal default values for all the settings
<F10>	Save changes and exit the UEFI SETUP UTILITY
<F12>	Print screen
<ESC>	Jump to the Exit Screen or exit the current screen

3.2 Main Screen

Once entering the UEFI SETUP UTILITY, the Main screen will appear and display the system overview. The Main screen provides system overview information and allows user to set the system time and date.



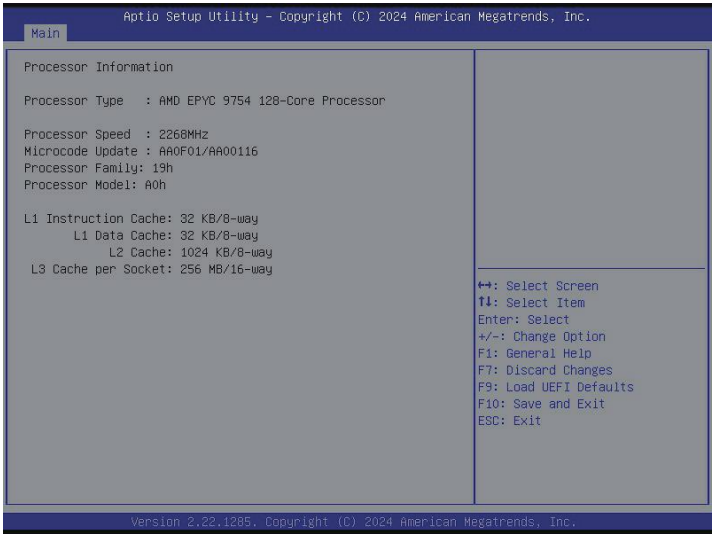
The screenshots in this manual are for references only. The actual images may slightly vary depending on the model and the version used.

3.2.1 Mother Board Information

Press <Enter> to view the information of the motheboard.

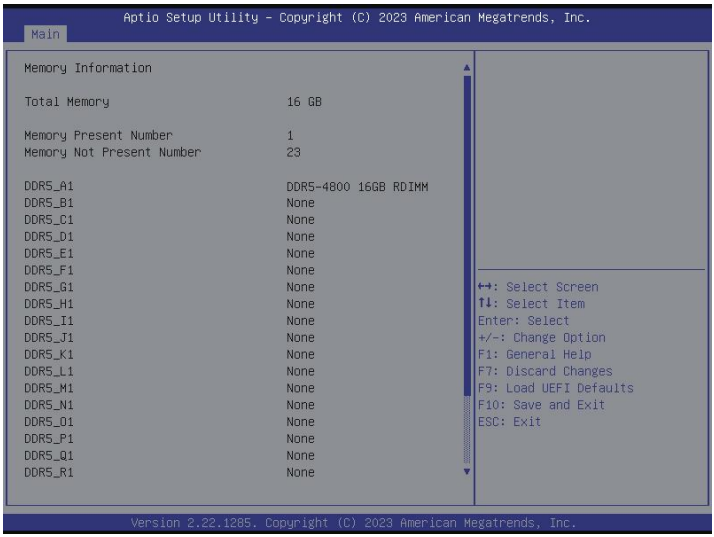
3.2.2 Processor Information

Press <Enter> to view the information of the processor.



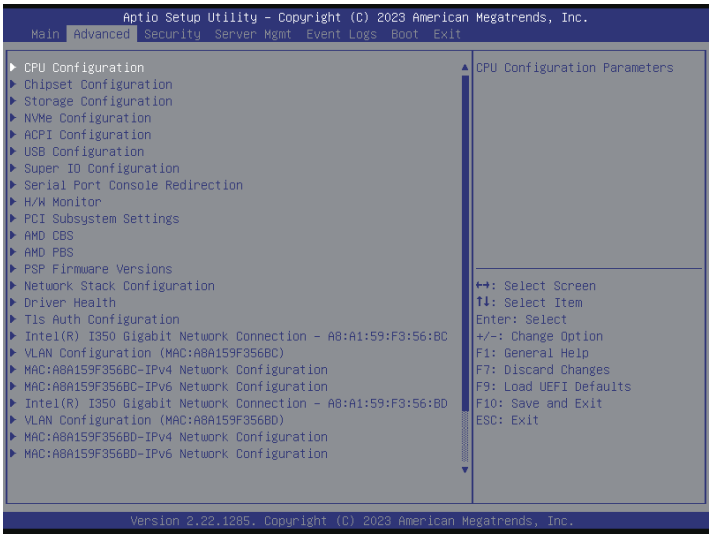
3.2.3 Memory Information

Press <Enter> to view the information of the memory.



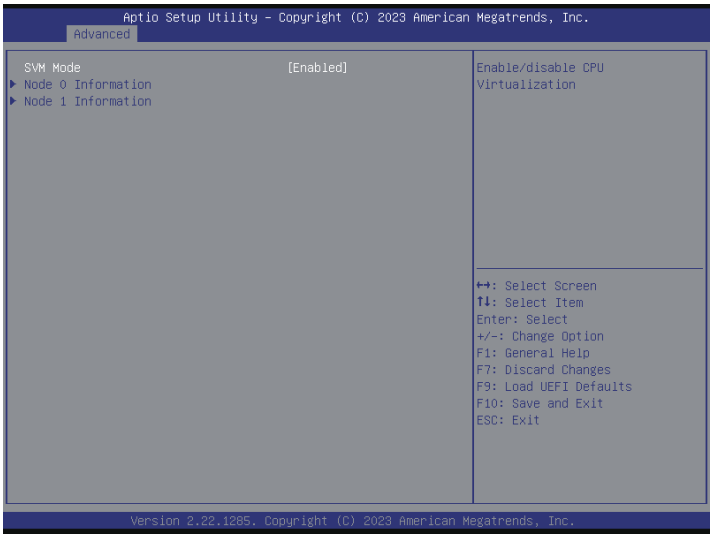
3.3 Advanced Screen

In this section, set the configurations for the following items: CPU Configuration, Chipset Configuration, Storage Configuration, NVMe Configuration, ACPI Configuration, USB Configuration, Super IO Configuration, Serial Port Console Redirection, H/W Monitor, PCI Subsystem Settings, AMD CBS, AMD PBS, PSP Firmware Versions, Network Stack Configuration, Driver Health, Tls Auth Configuration and Instant Flash.



Setting wrong values in this section may cause the system to malfunction.

3.3.1 CPU Configuration



SVM Mode

Enable or disable CPU Virtualization.

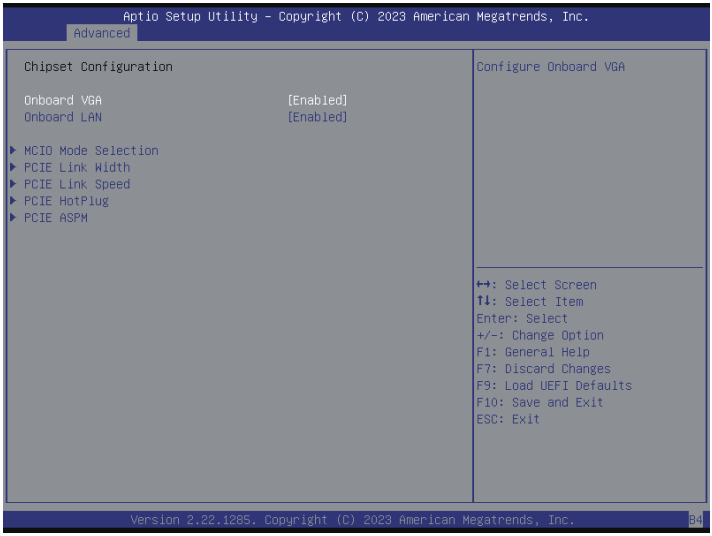
Node 0 Information

View Information related to Node 0.

Node 1 Information

View Information related to Node 1.

3.3.2 Chipset Configuration



Onboard VGA

Use this to enable or disable the Onboard VGA function.

Onboard LAN

Use this to enable or disable the Onboard LAN function.

MCIO Mode Selection

Select SATA or PCIE work in MCIO port.

MCIO7/8/17/18 Mode Selection
Select SATA or PCIE work in MCIO7/8/17/18 port.

PCIE Link Width

Select this item to configure PCIE Link Width.

MCIO1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20 Link Width
Select MCIO1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20 Link Width. The default value is [x4x4].

PCIE Link Speed

Select PCIE Link Speed.

MCIO9/10/19/20 Link Speed
Select MCIO9/10/19/20 Link Speed. The default value is [Auto].

PCIE HotPlug

Select this item to configure PCIE HotPlug globally.

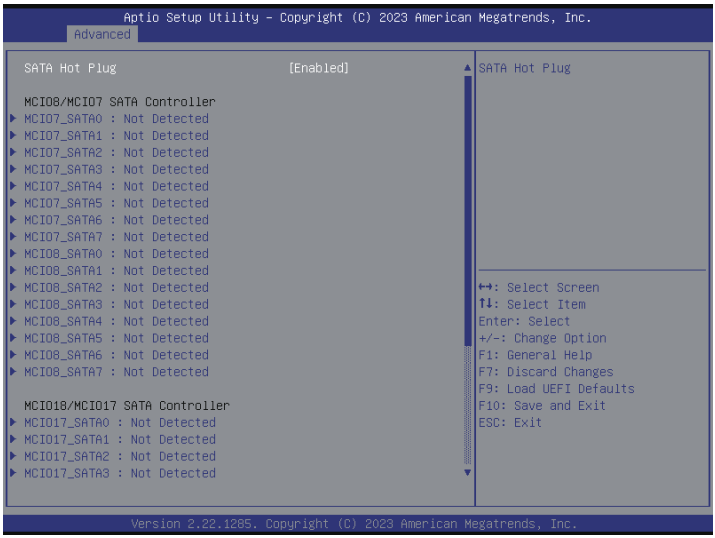
MCIO1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20 HotPlug
Enable or disable MCIO1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20 HotPlug.

PCIE ASPM

Selec this item to configure the PCIE ASPM.

PCI-E ASPM Support (Global)
Select this item to disable ASPM Support in all PCIE root ports.

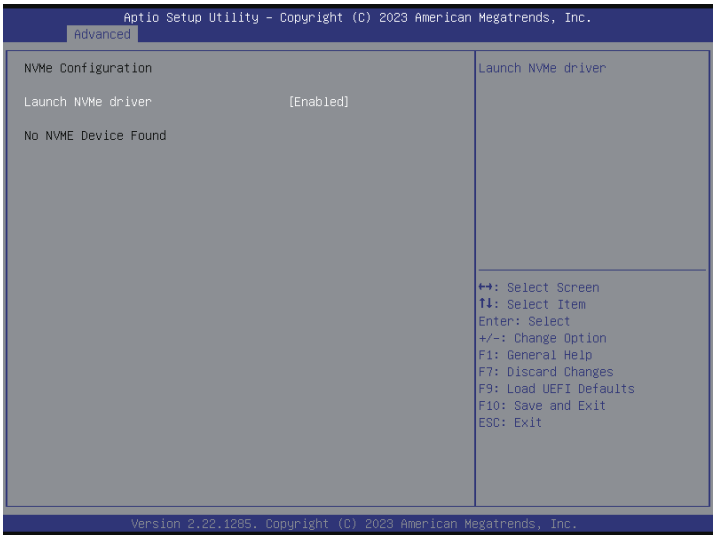
3.3.3 Storage Configuration



SATA Hot Plug

Use this item to enable or disable the SATA Hot Plug Function.

3.3.4 NVMe Configuration



The NVMe Configuration displays the NVMe Driver and Device information.

Launch NVMe driver

Use this item to enable or disable launch NVMe driver.

3.3.5 ACPI Configuration

PCIE Devices Power On

Allow the system to be waked up by a PCIE device and enable wake on LAN.

Ring-In Power On

Allow the system to be waked up by onboard COM port modem Ring-In Signals.

RTC Alarm Power On

Allow the system to be waked up by real time clock alarm. Set it to By OS to let it be handled by the operating system.

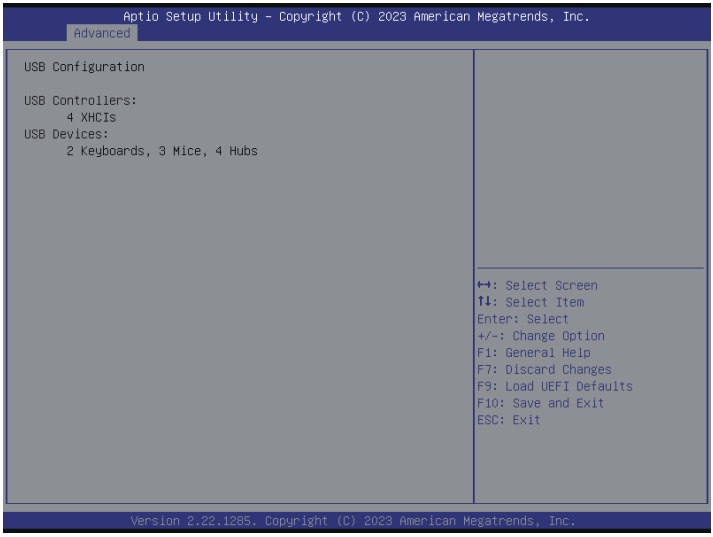
RTC Alarm Date
Set Date of RTC power on feature.

RTC Alarm Hour
Set Hour of RTC power on feature.

RTC Alarm Minute
Set Minute of RTC power on feature.

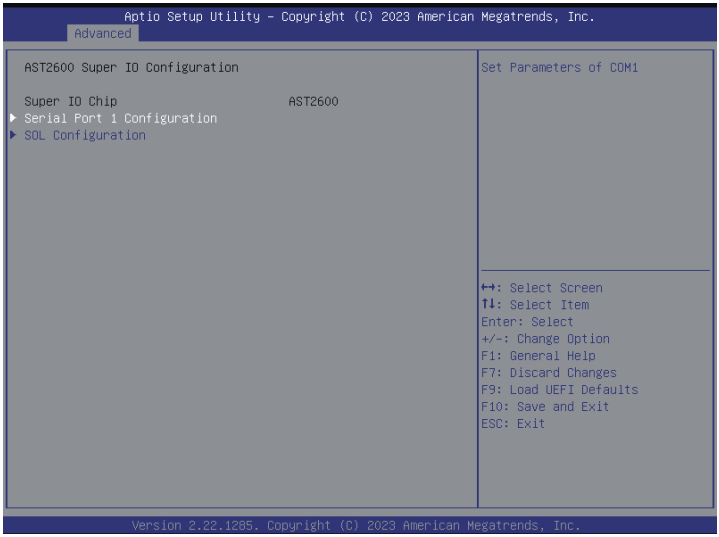
RTC Alarm Second
Set Second of RTC power on feature.

3.3.6 USB Configuration



This displays the USB Controllers and USB Devices information.

3.3.7 Super IO Configuration



Serial Port 1 Configuration

Use this item to set parameters of Serial Port 1 (COM1).

Serial Port

Use this item to enable or disable the Serial Port (COM).

Change Settings

Use this item to select an optimal setting for Super IO Device.

SOL Configuration

Use this item to set parameters of SOL.

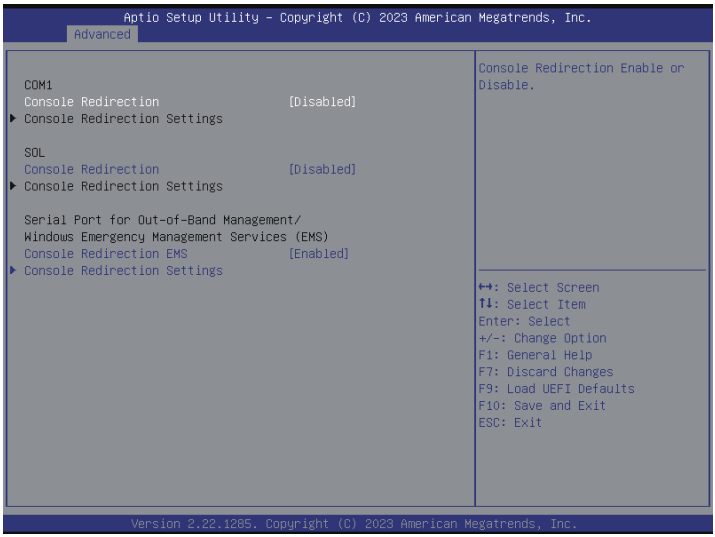
SOL Port

Use this item to enable or disable the SOL Port.

Change Settings

Use this item to select an optimal setting for Super IO Device.

3.3.8 Serial Port Console Redirection



COM1 / SOL

Console Redirection

Use this item to enable or disable Console Redirection. If this item is set to enable allowing to select a COM Port to be used for Console Redirection.

Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how the computer and the host computer to which are connected exchange information. Both computers should have the same or compatible settings.

Terminal Type

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100Plus	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

Bits Per Second
Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [38400], [57600] and [115200].

Data Bits
Use this item to set the data transmission size. The options include [7] and [8] (Bits).

Parity
Use this item to select the parity bit. The options include [None], [Even], [Odd], [Mark] and [Space].

Stop Bits
The item indicates the end of a serial data packet. The standard setting is [1] Stop Bit. Select [2] Stop Bits for slower devices.

Flow Control
Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None] and [Hardware RTS/CTS].

VT-UTF8 Combo Key Support
Use this item to enable or disable the VT-UTF8 Combo Key Support for ANSI/VT100 terminals.

Recorder Mode
Use this item to enable or disable Recorder Mode to capture terminal data and send it as text messages.

Resolution 100x31
Use this item to enable or disable extended terminal resolution support.

Putty Keypad
Use this item to select Function Key and Keypad on Putty.

Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS)

Console Redirection EMS

Use this option to enable or disable Console Redirection. If this item is set to Enabled, user can select a COM Port to be used for Console Redirection.

Console Redirection Settings

Use this option to configure Console Redirection Settings, and specify how the computer and the host computer to which are connected exchange information.

Out-of-Band Mgmt Port

Microsof t Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

Terminal Type EMS

Use this item to select the preferred terminal emulation type for out-of-band management. It is recommended to select [VT-UTF8].

Option	Description
VT100	ASCII character set
VT100+	Extended VT100 that supports color and function keys
VT-UTF8	UTF8 encoding is used to map Unicode chars onto 1 or more bytes
ANSI	Extended ASCII character set

Bits Per Second EMS

Use this item to select the serial port transmission speed. The speed used in the host computer and the client computer must be the same. Long or noisy lines may require lower transmission speed. The options include [9600], [19200], [57600] and [115200].

Flow Control EMS

Use this item to set the flow control to prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to restart the flow. Hardware flow uses two wires to send start/stop signals. The options include [None], [Hardware RTS/CTS], and [Software Xon/Xoff].

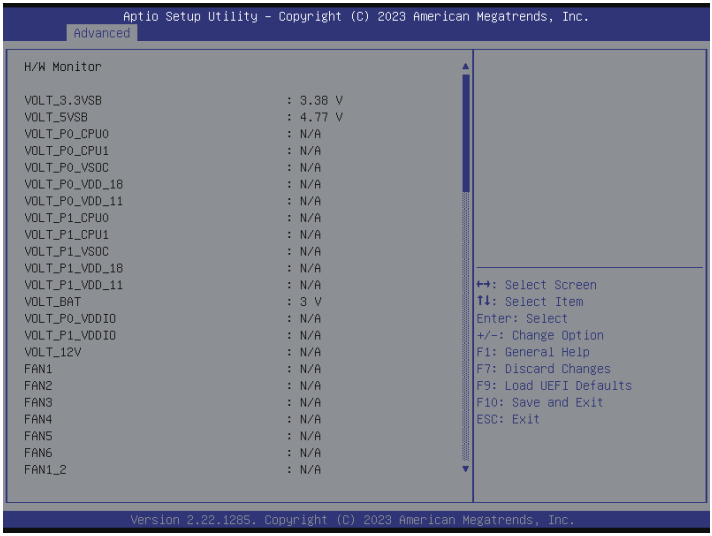
Data Bits EMS

Parity EMS

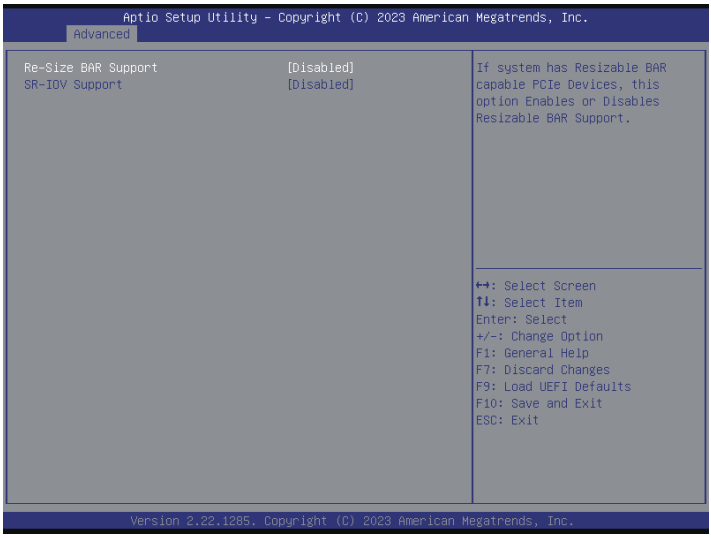
Stop Bits EMS

3.3.9 H/W Monitor

In this section, it allows user to monitor the status of the hardware on the system, including the parameters of the CPU temperature, motherboard temperature, CPU fan speed, chassis fan speed, and the critical voltage.



3.3.10 PCI Subsystem Settings



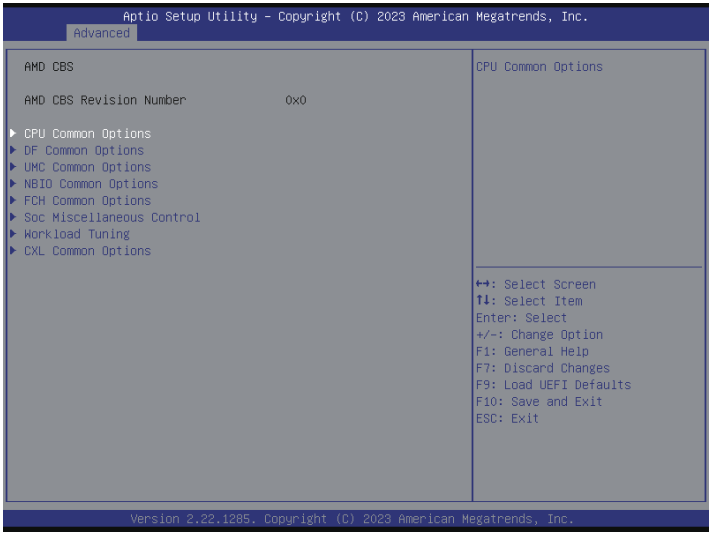
Re-Size BAR Support

Enable or disable this item to Re-Size BAR supported upon the sysem has resizable BAR capable PCIe Devices.

SR-IOV Support

If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.

3.3.11 AMD CBS



CPU Common Options

Use this item to configure CPU Common options.

DF Common Options

Use this item to configure DF Common options.

UMC Common Options

Use this item to configure UMC Common options.

NBIO Common Options

Use this item to configure NBIO Common options.

FCH Common Options

Use this item to configure FCH Common options.

Soc Miscellaneous Control

Use this item to configure Soc Miscellaneous Control options.

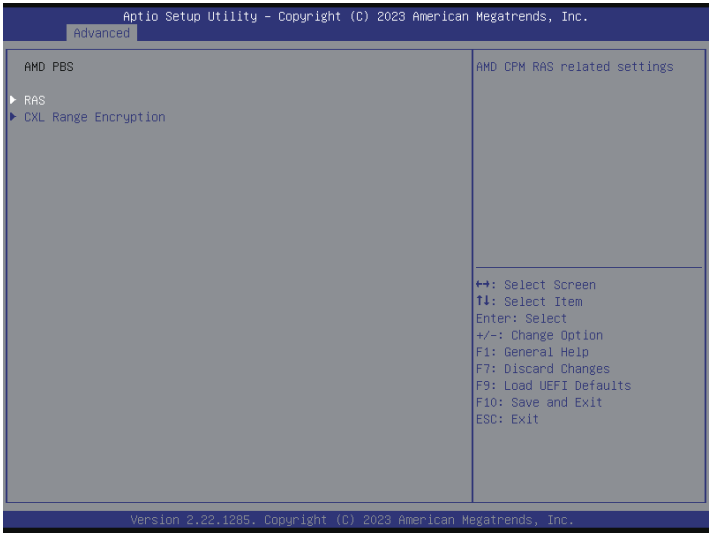
Workload Tuning Options

Use this item to configure Workload Tuning options.

CXL Common Options

Use this item to configure CXL Common options.

3.3.12 AMD PBS



RAS

Use this item to configure AMD CPM RAS related settings.

RAS Periodic SMI Control
Use this to enable or disable Periodic SMI for polling [MCA Threshold] error.

SMI Threshold
This limits the number of [MCA Threshold and Deferred Error SMI source] per a unit time.

SMI Scale
Use this to define the time scale.

SMI Scale Unit
Use this to define the unit of time scale.

SMI Period
Use this to define the polling interval with ms unit. Input 0 value to disable this function.

GHES Notify Type
This specifies the notification type for deferred/corrected errors.

GHES UnCorr Notify Type
This specifies the notification type for uncorrected errors.

PCIe GHES Notify Type
This specifies the notification type for PCIe corrected errors.

PCIe UnCorr GHES Notify Type
This specifies the notification type for PCIe uncorrected errors.

PCIe Root Port Corr Err Mask Reg
Use this to initialize the PCIe AER corrected error mask register of root port.

PCIe Root Port UnCorr Err Mask Reg
Use this to initialize the PCIe AER uncorrected error mask register of root port.

PCIe Root Port UnCorr Err Sev Reg
Use this to initialize the PCIe AER uncorrected error severity registers of root port.

PCIe Device Corr Err Mask Reg
Use this to initialize the PCIe AER corrected error mask register of PCIe device.

PCIe Device UnCorr Err Mask Reg
Use this to initialize the PCIe AER uncorrected error mask register of PCIe device.

PCIe Device UnCorr Error Sev Reg
Use this to initialize the PCIe AER uncorrected error severity registers of PCIe device

CXL DP CIE Mask Enable
Use this to enable or disable masking of CXL DP correctable error-internal error.

DRAM Hard Post Package Repair
Use this to enable or disable the spare DRAM rows to replace malfunctioning rows via an in-field repair mechanism.

HEST DMC Structure Support
Use this to enable or disable HEST DMC (Deffered Maching Check) structure support.

CXL Error Report Support
Use this to enable or disable CXL error reporting.

CXL Range Encryption

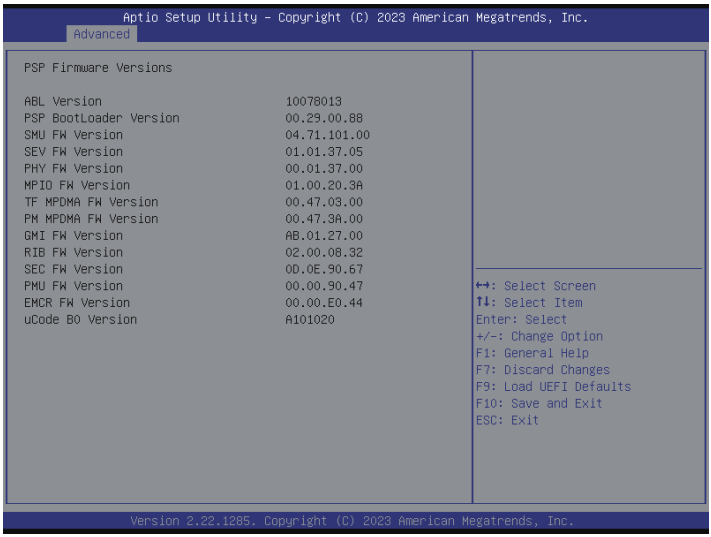
Configure AMD CXL range encryption setting.

Range 1/2/3/4/5/6/7 Memory Base
Use this item to enter memory range base address.

Range 1/2/3/4/5/6/7 Memory Limit
Use this item to enter memory range limit address.

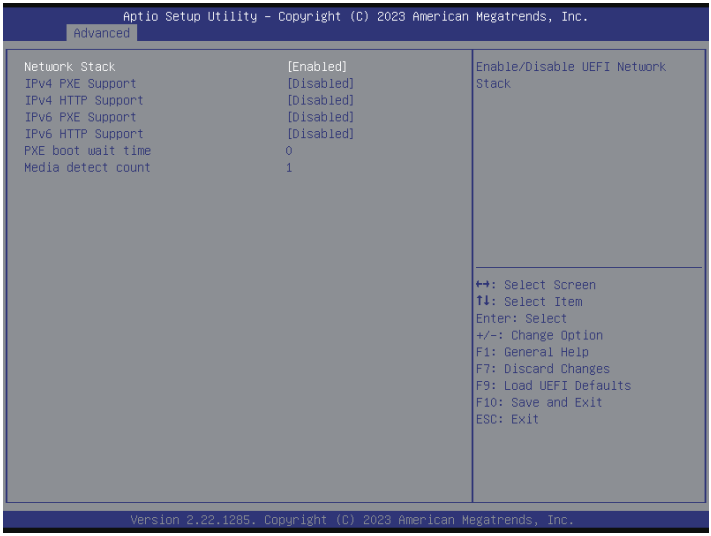
Start CXL Range Encryption
Use this to encrypt all memory ranges.

3.3.13 PSP Firmware Versions



The PSP Firmware Verions displays the version information of ABL, PSP BootLoader, SMU FW, SEV FW, PHY FW, MPIO FW, TF MPDMA FW, PM MPDMA FW, GMI FW, RIB FW, SEC FW, PMU FW, EMCR FW and uCode B0.

3.3.14 Network Stack Configuration



Network Stack

Use this item to enable or disable UEFI Network Stack.

IPv4 PXE Support

Use this to enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

IPv4 HTTP Support

Use this to enable or disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.

IPv6 PXE Support

Use this to enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

IPv6 HTTP Support

Use this to enable or disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.

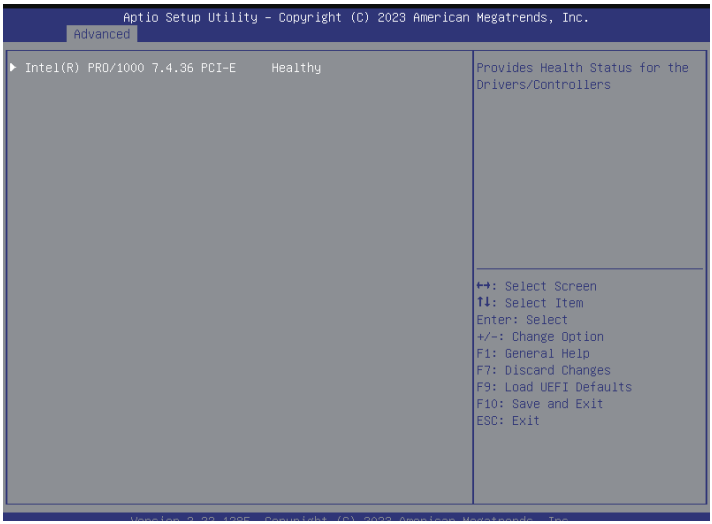
PXE boot wait time

Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

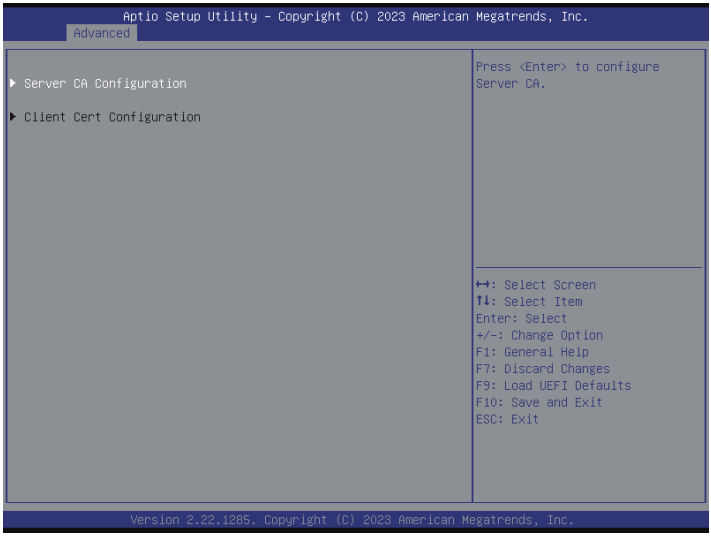
3.3.15 Driver Health



Inter(R) PRO/1000 7.4.36 PCI-E Healthy

Provides Health Status for the Drivers/Controllers.

3.3.16 Tls Auth Configuration



Server CA Configuration

Press <Enter> to configure Server CA.

Enroll Cert

Press <Enter> to enroll cert.

Delete Cert

Press <Enter> to delete cert.

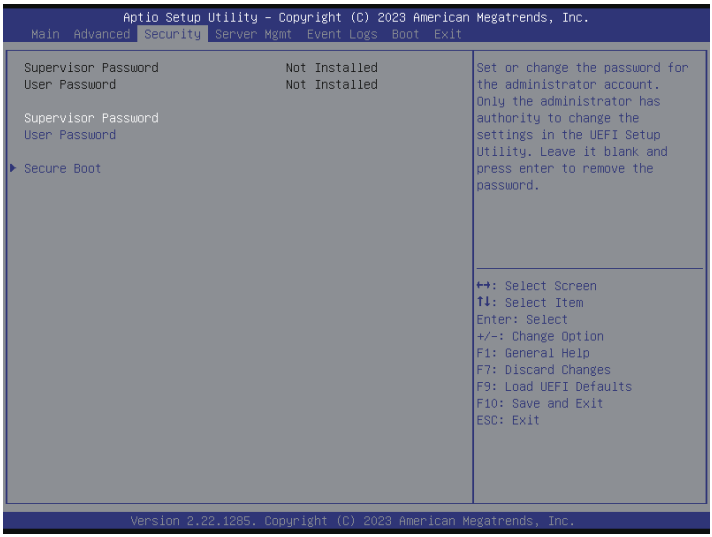
Client Cert Configuration

3.3.17 Instant Flash

Instant Flash is a UEFI flash utility embedded in Flash ROM. This convenient UEFI updatetool allows user to update system UEFI without entering operating systems first like MSDOS or Windows®. Just save the new UEFI file to the USB flash drive, floppy disk or hard drive and launch this tool, then update the UEFI only in a few clicks without preparing an additional floppy diskette or other complicated flash utility. Please be noted that the USB flash drive or hard drive must use FAT32/16/12 file system. Execute the Instant Flash utility, the utility will show the UEFI files and the respective information. Select the proper UEFI file to update UEFI, and reboot the system after the UEFI update process is completed.

3.4 Security

This section allows user to set or change the supervisor/user password for the system. For the user password item is allowed user to clear it.



Supervisor Password

Set or change the password for the administrator account. Only the administrator has authority to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

User Password

Set or change the password for the user account. Users are unable to change the settings in the UEFI Setup Utility. Leave it blank and press enter to remove the password.

Secure Boot

Use this to enable or disable Secure Boot Control. The default value is [Disabled]. Enable to support Windows Server 2012 R2 or later versions Secure Boot.

Secure Boot Mode

Secure Boot mode selector: Standard/Custom. In Custom mode Secure Boot Variables can be configured without authentication.

Install Default Secure Boot Keys

Please install default secure boot keys if it's the first time to use secure boot.

Clear Secure Boot Keys

This force system to setup Mode-Clear all Secure Boot Variables. Change takes effect after reboot.

3.4.1 Key Management

In this section, expert users can modify Secure Boot Policy variables without full authentication.

Factory Key Provision

Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.

Install Default Secure Boot Keys

Please install default secure boot keys if it's the first time to use secure boot.

Clear Secure Boot Keys

This force system to setup Mode-Clear all Secure Boot Variables. Change takes effect after reboot.

Enroll Efi Image

Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db).

Export Secure Boot Variables

Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.

Platform Key (PK)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, External, Mixed

Key Exchange Keys (KEK)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, External, Mixed

Authorized Signatures (db)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, External, Mixed

Forbidden Signatures (dbx)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, External, Mixed

Authorized TimeStamps (dbt)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, External, Mixed

OsRecovery Signatures (dbr)

Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:

a) EFI_SIGNATURE_LIST

b) EFI_CERT_X509 (DER)

c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHAXXX

2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)

Key Source: Factory, External, Mixed

3.5 Server Mgmt

Wait For BMC

Wait For BMC response for specified time out. BMC starts at the same time when BIOS starts during AC power ON. It takes around 255 seconds to initialize Host to BMC interfaces.

FRB-2 Timer

Use this item to enable or disable FRB-2 timer (POST timer)

FRB-2 Timer Timeout

Use this to define the FRB-2 Time Expiration between 1 to 30 value.

FRB-2 Timer Policy

Configure how the system should respond. If the FRB-2 Timer expires is disabled, this item is not available.

OS Watchdog Timer

Use this item to enable or disable OS Watchdog Timer. If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads.

OS Wtd Timer Timeout

Configure the OS Boot Watchdog Timer Expiration between 1 to 30 min value. If the OS Boot Watchdog Timer is disabled, this item is not available.

OS Wtd Timer Policy

Configure how the system should respond if the OS Boot Watchdog Timer expires. If the OS Boot Watchdog Timer is disabled, this item is not available.

BMC Network Configuration

Use this to configure BMC network parameters.

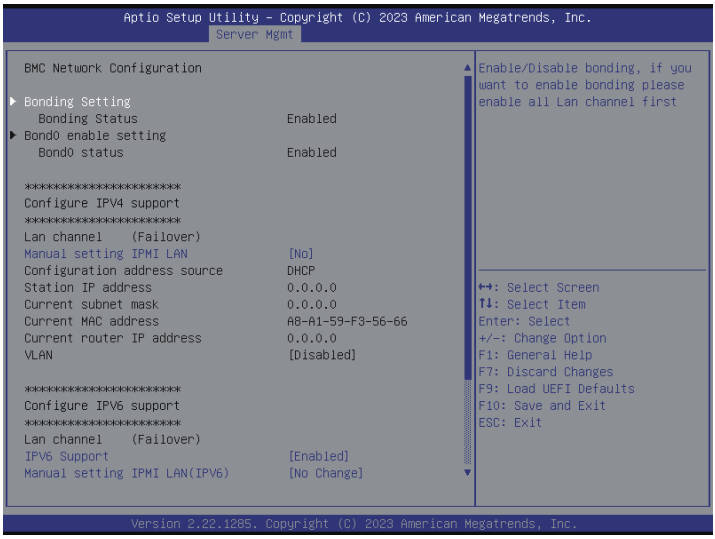
System Event Log

Press <Enter> to change the SEL event log configuration.

BMC Tools

Use this item to configure about KCS control, restore AC power loss and load BMC default setings.

3.5.1 BMC Network Configuration



Bonding Setting

Select this item to enabled or disabled bonding. Please enable all lan channel first when want to enable bonding.

Lan channel (Failover)

Manual Setting IPMI LAN

If [No] is selected, the IP address is assigned by DHCP. If using a static IP address, toggle to [Yes], and the changes take effect after the system reboots. The default value is [No].

Configuration Address Source

Select to configure BMC network parameters statically or dynamically(by BIOS or BMC). Configuration options: [Static] and [DHCP].

Static: Manually enter the IP Address, Subnet Mask and Gateway Address in the BIOS for BMC LAN channel configuration.
DHCP: IP address, Subnet Mask and Gateway Address are automatically assigned by the network's DHCP server.

The default login information for the IPMI web interface is:
Username: admin
Password: admin

For more instructions on how to set up remote control environment and use the IPMI management platform, please refer to the IPMI Configuration User Guide or go to the Support website at: http://www.asrockrack.com/support/faq.asp

VLAN

Enable or disable Virtual Local Area Network.

If [Enabled] is selected, configure the items below.

VLAN ID: Select this item to configure the VLAN ID setting, the Maximum value is 4094 and the Minimum value is 1.

VLAN Priority: Select this item to configure the VLAN Priotity setting. the Maximum value is 7 and the Minimum value is 0.

IPV6 Support

Enable or disable LAN IPV6 Support.

Manual Setting IPMI LAN(IPV6)

Select to configure LAN channel parameters statically or dynamically(by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.

3.5.2 System Event Log

SEL Components

Change this to enable or disable event logging for error/progress codes during boot.

Erase SEL

Use this to choose options for earsing SEL.

When SEL is Full

Use this to choose options for reactions to a full SEL.

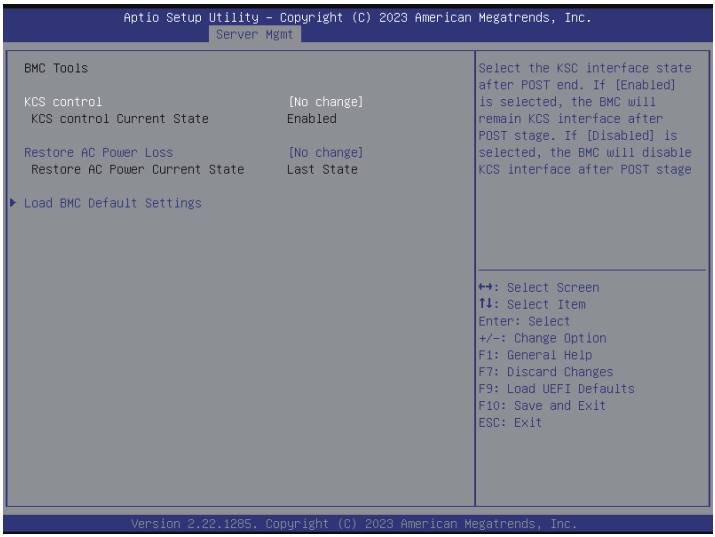
Log EFI Status Codes

Use this item to disable the logging of EFI Status Codes or log only error code or only progress code or both.

PCIe Device Degrade ELog Support

Use this item to enable or disable PCIe Device Degrade Error Logging Support.

3.5.3 BMC Tools



KCS Control

Select this KCS interface state after POST end. If [Enabled] us selected, the BMC will remain KCS interface after POST stage. If [Disabled] is selected, the BMC will disable KCS interface after POST stage

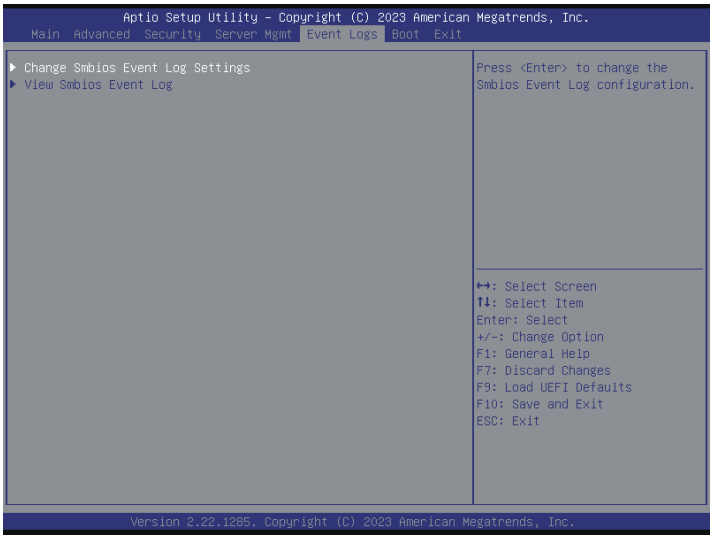
Restore AC Power Loss

This allows user to set the power state after an unexpected AC/power loss. If [Power Off] is selected, the AC/power remains off when the power recovers. If [Power On] is selected, the AC/power resumes and the system starts to boot up when the power recovers. If [Last State] is selected, it will recover to the state before AC/power loss.

Load BMC Default Settings

Use this item to Load BMC Default Settings

3.6 Event Logs



Change Smbios Event Log Settings

Use this item to configure the Smbios Event Log Settings.
When entering the item, the screen displays following sub-items:

Smbios Event Log
Use this item to enable or disable all features of the SMBIOS Event Logging during system boot.

Erase Event Log
Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.

When Log is Full
Use this item to choose options for reactions to a full Smbios Event Log. The options include [Do Nothing] and [Erase Immediately].

Log System Boot Event
Choose option to enable/disable logging of System boot event.

MECI (Multiple Event Count Increment)
Use this item to enter the increment value for the multiple event counter. The valid range is from 1 to 255.

METW (Multiple Event Time Window)
Use this item to specify the number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.

Log EFI Status Code
Enable or disable the logging of EFI Status Codes as OEM reserved type E0 (if not already converted to legacy).

Convert EFI Status Codes to Standard Smbios Type
Enable or disable the converting of EFI Status Codes to Standard Smbios Types (Not all may be translated).

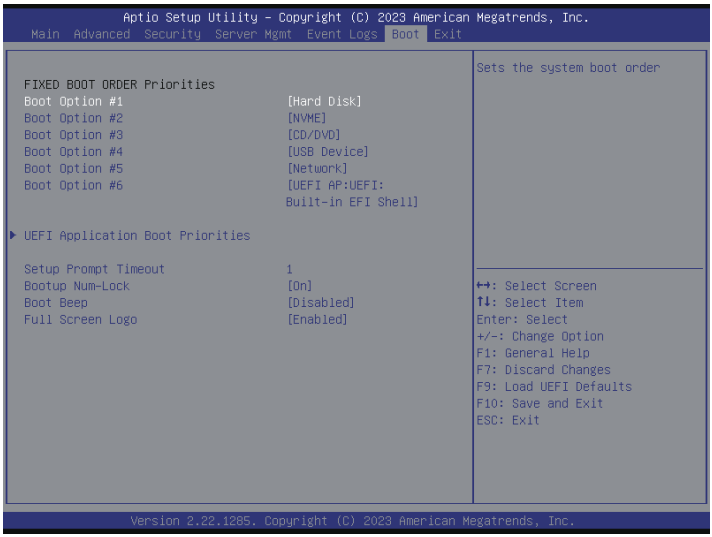
View Smbios Event Log

Press <Enter> to view the Smbios Event Log records.

All values changed here do not take effect until computer is restarted.

3.7 Boot Screen

In this section, it will display the available devices on the system for user to configure the boot settings and the boot priority.



Boot Option #1/#2/#3/#4/#5/#6

Use this to set the system boot order.

UEFI Application Boot Priorities

Specifies the Boot Device Priority sequence from available UEFI Application.

Setup Prompt Timeout

Configure the number of seconds to wait for the UEFI setup utility.

Bootup Num-Lock

Select whether Num Lock should be turned on or off when the system boots up.

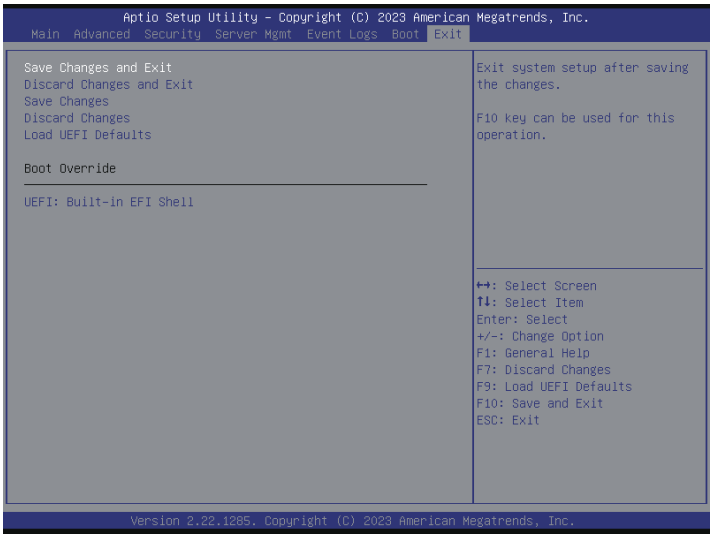
Boot Beep

Select whether the Boot Beep should be turned on or off when the system boots up. Please note that a buzzer is needed.

Full Screen Logo

Enable to display the boot logo or disable to show normal POST message.

3.8 Exit Screen



Save Changes and Exit

When selecting this option, the following message “Save configuration changes and exit setup?” will pop-out. Press <F10> key or select [Yes] to save the changes and exit the UEFI SETUP UTILITY.

Discard Changes and Exit

When selecting this option, the following message “Discard changes and exit setup?” will pop-out. Press <ESC> key or select [Yes] to exit the UEFI SETUP UTILITY without saving any changes.

Save Changes

When selecting this option, the following message “Save changes?” will pop-out. Select [Yes] to save all changes.

Discard Changes

When selecting this option, the following message “Discard changes?” will pop-out. Select [Yes] to discard all changes.

Load UEFI Defaults

Load UEFI default values for all the setup questions. F9 key can be used for this operation.

Chapter 4 Software Support

After all the hardware has been installed, it suggests to go to the offical website at http://www.ASRockRack.com and make sure if there are any new updates of the BIOS / BMC firmware for the motherboard.

4.1 Download and Install Operating System

This motherboard supports various Microsoft® Windows® Server / Linux compliant operating systems. Please download the operating system from the OS manufacturer. Please refer to the OS documentation for more instructions.

** Please download the Intel® SATA Floppy Image driver from the ASRock Rack's website (www.asrockrack.com) to the USB drive while installing OS in SATA RAID mode.*

4.2 Download and Install Software Drivers

This motherboard supports various Microsoft® Windows® compliant drivers. Please download the required drivers from the website at http://www.ASRockRack.com.

To download necessary drivers, go to the product page, click on the "Download" tab, choose the operating system that is used, and then download the using driver.

4.3 Contact Information

Contact ASRock Rack or want to know more about ASRock Rack, welcome to visit ASRock Rack's website at http://www.ASRockRack.com; or contact the dealer for further information.

Chapter 5 Troubleshooting

5.1 Troubleshooting Procedures

Follow the procedures below to troubleshoot the system.

Always unplug the power cord before adding, removing or changing any hardware components. Failure to do so may cause physical injuries and damages to motherboard components.

1. Disconnect the power cable and check whether the PWR LED is off.
2. Unplug all cables, connectors and remove all add-on cards from the motherboard. Make sure that the jumpers are set to default settings.
3. Confirm that there are no short circuits between the motherboard and the chassis.
4. Install a CPU and fan on the motherboard, then connect the chassis speaker and power LED.

If there is no power...

1. Confirm that there are no short circuits between the motherboard and the chassis.
2. Make sure that the jumpers are set to default settings.
3. Check the settings of the 115V/230V switch on the power supply.
4. Verify if the battery on the motherboard provides ~3VDC. Install a new battery if it does not.

If there is no video...

1. Try replugging the monitor cables and power cord.
2. Check for memory errors.

If there are memory errors...

1. Verify that the DIMM modules are properly seated in the slots.
2. Use recommended DDR5 RDIMM/RDIMM-3DS
3. Install more than one DIMM modules that should be identical with the same brand, speed, size and chip-type.
4. Try inserting different DIMM modules into different slots to identify faulty ones.
5. Check the settings of the 115V/230V switch on the power supply.

Unable to save system setup configurations...

1. Verify if the battery on the motherboard provides ~3VDC. Install a new battery if it does not.
2. Confirm whether the power supply provides adaquate and stable power.

Other problems...

1. Try searching keywords related to the related problem on ASRock Rack's FAQ page: http://www.asrockrack.com/support

5.2 Technical Support Procedures

If the problems are still unsolved, please contact ASRock Rack's technical support with the following information:

1. Contact information
2. Model name, BIOS version and problem type.
3. System configuration.
4. Problem description.

Contact ASRock Rack's technical support at:
http://www.asrockrack.com/support/tsd.asp

5.3 Returning Merchandise for Service

For warranty service, the receipt or a copy of the invoice marked with the date of purchase is required. By calling the vendor or going to RMA website (http://event. asrockrack.com/tsd.asp) to obtain a Returned Merchandise Authorization (RMA) number.

The RMA number should be displayed on the outside of the shipping carton which is mailed prepaid or hand-carried when returning the motherboard to the manufacturer. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty does not cover damages incurred in shipping or from failure due to alteration, misuse, abuse or improper maintenance of products.

Contact the distributor first for any product related problems during the warranty period.

Contact Information

If it needs to contact ASRock Rack or want to know more about ASRock Rack, you're welcome to visit ASRock Rack's website at http://www.asrockrack.com; or contact the dealer for further information. For technical questions, please submit a support request form at https://event.asrockrack.com/tsd.asp

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